C13-R3: DIGITAL SYSTEM DESIGN

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) What is multiplexer? Justify whether a multiplexer is sufficient to realize any Boolean function.

b) Simplify the following Boolean expression, and also obtain the simplified expression in POSs form.

$$F = (C+D)' + A'CD' + AB'C' + A'B'CD + ACD'$$

c) Realize a 3-input XOR gate with the help of 2-input NAND gates only.

d) Relatively compare the advantages and disadvantages of synchronous counter and asynchronous counter.

e) Differentiate demultiplexer from decoder.

f) What is ripple counter? "Ripple counter is also known as divided-by-*n* counter." - Explain.

g) Obtain a clocked T flip-flop using a clocked D flip-flop as basic unit.

(7x4)

2.

a) Draw a logic circuit of a 4-bit shift register with the help of JK flip-flops and multiplexers having the facilities of (i) parallel loading, (ii) right shifting, (iii) left shifting, and (iv) no change. Clearly state how are the facilities achieved.

b) Design a clocked JK flip-flop using only NAND gates.

c) Define race problem. What do you mean by race-around condition? Devise a mechanism to resolve it and clearly state how it operates.

(6+6+6)

3.

a) State Shannon's Expansion Theorem, and prove it.

b) Define minterm and maxterm. Give an example of each. State their significance, and explain why they are so called.

c) Suppose a decade counter is used to count down from 9 through 0. Design a combinational circuit, using only basic gates, that is to be appended after the decade counter, so that the overall circuitry behaves like a down counter.

(6+6+6)

4.

a) Prove that NAND and NOR gates are universal logic gates.

b) Describe the general structure of CMOS logic circuit. Obtain the transistor level circuit of CMOS 3-input OR gate.

c) Design a CMOS circuit for the full adder, where (i) A_n, B_n, and C_n are three input variables, (ii) Output carry C_{n+1} is a function of A_n, B_n, and C_n, and (iii) Output sum S_n is a function of A_n, B_n, C_n, and C_{n+1}.

(4+6+8)

5.

a) A synchronous counter with four JK flip-flops has the following connections.

$J_A = K_A = 1$,

$J_B = Q_A \cdot Q_D'$, $K_B = Q_A$,

$J_C = K_C = Q_A \cdot Q_B$,

$J_D = Q_A \cdot Q_B \cdot Q_C$, and $K_D = Q_A$

Determine the modulus, *n* of the counter, and draw the output waveforms of the same.

b) Realize the CMOS circuit with its structural specification as given below. The circuit consists of four transistors in series, two consecutive pMOS transistors Q_1 and Q_2 with the source of Q_1 as V_{DD}, two consecutive nMOS transistors Q_3 and Q_4 with the source of Q_4 as grounded, and the output at the common drain of Q_2 and Q_3. In addition, the gates of Q_1 and Q_4 are common to input 1, whereas the gates of Q_2 and Q_3 are complementary to each other, with the gate of Q_2 as input 2.

c) Draw the circuit diagram of a three-input totem-pole output TTL NAND gate. State with justification whether two or more totem-pole outputs can be wire-ANDed.

(9+5+4)

6.

a) Design a serial two's complementer circuit using JK flip-flop as the basic memory element.

b) What is PLD? Write a short note on PLA folding.

c) Mention the advantages and disadvantages of Gate Array design style over Custom (or Semi-Custom) design style, in designing VLSI chips.

(7+5+6)

7.

a) Construct a sequence generator to produce the sequence 11010110.

b) Design a synchronous counter using JK flip-flops to count the sequence:

"1-3-15-5-8-2-0-12-6-9"

c) Write a short note on Data flow modeling of VHDL.

(6+8+4)