C13-R3: DIGITAL SYSTEM DESIGN

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) The following calculation was performed by a particular breed of unusually intelligent chicken. If the radix r used by the chicken corresponds to its total number of toes, how many toes does the chicken have on each foot?

$((35)_r + (24)_r) \times (21)_r = (1501)_r$

b) Prove that the dual of the exclusive-OR is also its complement.

c) Design a combinational circuit that multiplies by 5 an input decimal digit represented in BCD. The output is also in BCD. Show that the outputs can be obtained from the input lines without using any logic gates.

d) Define programmable Array Logic (PALs). How are they characterized?

e) In VHDL, there are two types of delay that can be used for modelling behaviour. Taking a suitable example, explain each of them in brief.

f) Datapaths provide connections between components in the system and are classified according to different features. Explain each feature of the datapath in brief.

g) Which are the programmable elements of FPGA module? Explain the functions of each of them in brief.

(7x4)

2.

a) Implement the four Boolean functions listed using three half-adder circuits

$D = A \oplus B \oplus C$

$E = \overline{A}BC + A\overline{B}C$

$F = AB\overline{C} + (\overline{A} + \overline{B})C$

$G = ABC$

b) A combinational circuit is specified by the following three Boolean functions:

$F_1 = \overline{X + Y} + XY\overline{Z}$

$F_2 = \overline{X + Y} + \overline{X}YZ$

$F_3 = XYZ + \overline{X + Y}$

Design the circuit with a decoder and external OR gates.

c) Design a synchronous mod-6 counter whose counting sequence is 000, 010, 011, 110, 101, 001, 000 etc. Use clocked JK flip-flops.

(4+4+10)

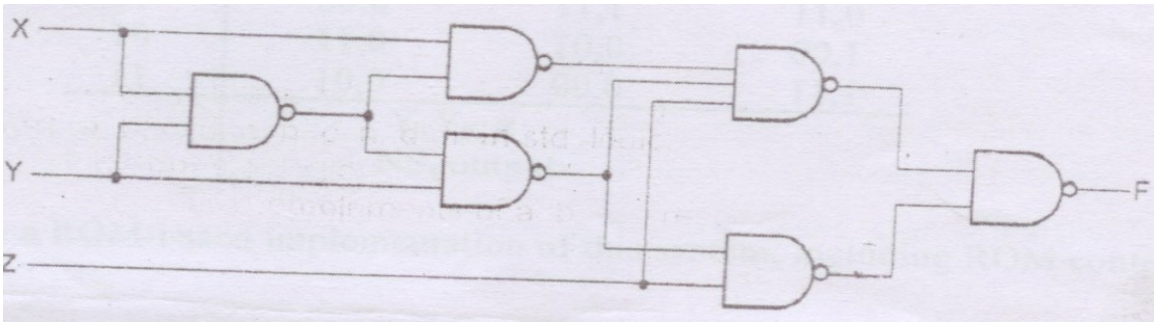
3.

a) Find a logic diagram representing minimum 2-level logic needed to implement the VHDL dataflow description give below. Note that complemented inputs are available.

```
-- Combinational Circuit 2: Dataflow VHDL Description
- library ieee;
use ieee. std_logic_1164. all;
entity comb_ckt_2 is
        port (a, b, c, d, a_n, c_n, d_n: in std_logic;
                f, g: out std_logic);
-- a_n, b_n, .. are complements of a, b, …, respectively.
end comb_ckt_2;
```

```
architecture dataflow_1 of comb_ckt_2 is
begin
f <= b and (a or (a_n and c)) or (b_n and c and d_n);
g <= b and (c or (a_n and c_n)) or (c_n and d_n);
end dataflow_1;
```

b) Write a dataflow description for the circuit in Figure given below by using the Boolean equation for the output F.



(9+9)

4.

a) Simulate the 4 x 1 MUX using Behavioral Style Modeling.

b) For the following expressions:

$f_1 (x, y, z) = \Sigma m (1, 2, 4, 5, 7)$

$f_2 (x, y, z) = \Sigma m (0, 1, 3, 5, 7)$

Illustrate the use of PAL to realize combinational logic.

(9+9)

5.

a) A sequential circuit with two D flip-flops A and B, two inputs X and Y, and one output Z is specified by the following input equations:

$D_A = \overline{X}Y + XA \qquad D_B = \overline{X}B + XA \qquad Z = XB$

i) Draw the logic diagram of the circuit.

ii) Derive the state table

iii) Derive the state diagram

b) A one-digit BCD adder using FPGA module is to be designed. Write high-level specifications of the system. Draw a scheme that uses two binary adders. Show the steps only for FPGA implementation.

(9+9)

6.

a) ROM modules can be classified according to the way that their contents (the values of the constant bit-vectors) are set. Explain this classification and discuss the advantages and disadvantages of each of them.

b) Consider sequential system described by the following tabular representation (the combination $x_1x_0 = 00$ never appears, so it is considered a don't care case):

Input: $\underline{x} = (x_1, x_0), x_i \in \{0, 1\}$

Output: $z \in \{0, 1\}$

State: $\underline{y} = (y_1, y_0), y_i \in \{0, 1\}$

Function: The transition and output function are

PS	x_1x_0		
y_1y_0	01	10	11
00	01,0	10,1	10,0
01	00,0	11,1	11,0
10	11,0	10,0	00,1

11	10,0	00,0	11,1

Show a ROM-based implementation of this system, including ROM contents.

(8+10)

7.

a) ASM (Algorithmic State Machine) is a controller for the logic design of a digital system and is regarded as a hardware algorithm. Show the general model of an ASM and explain the working of each functional block.

b) Consider a design example of a parallel (unsigned) 4-bit binary multiplier.

   i) Draw a possible system architecture diagram for the binary multiplier, showing different components, which are required for the design.

   ii) Mention the signals associated with its controller and draw an ASM chart for the same.

(6+12)