AMIETE – ET (OLD SCHEME)

Code: AE27 **Subject: DIGITAL HARDWARE DESIGN**
Time: 3 Hours **Max. Marks: 100**

DECEMBER 2009

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2x10)

a. The outputs of a system at any time are determined from present inputs and previous stored values in _____.

(A) Combinational system
(B) Sequential system
(C) RTL system
(D) None of above

b. Modeling a digital design as a set of components and interconnections is done in _____.

(A) Data flow design **(B)** Behavioural design
(C) Mixed style design **(D)** Structural design

c. The Boolean algebra expression $(x + x')y =$

(A) x **(B)** y
(C) x+y **(D)** $x' + y$

d. In _____ state machine, output is a function of _____ and _____.

(A) Mealy, present-state, external inputs
(B) Moore, present-state, external inputs
(C) Mealy, next-state, external inputs
(D) Moore, next-state, external inputs

e. A Programmable Array Logic (PAL) has

(A) Hardwired AND array and a programmable OR array
(B) Hardwired OR array and a programmable AND array
(C) Programmable AND array and a programmable OR array
(D) Hardwired AND array and a hardwired OR array

f. What is value of base r if $(121)_r = (144)_8$?

(A) 7 **(B)** 8

(C) 9 **(D)** 10

g. The circuit shown in Fig. 1 detects the following sequence

(A) 0001 **(B)** 0111
(C) 0101 **(D)** 1111

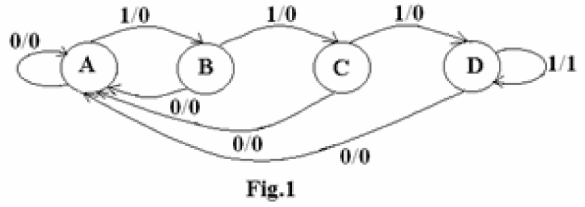

Fig.1

h. The threshold element shown in Fig.2, realises the switching function, where Y= f (x1,x2,x3)

(A) Y = Σ (1,2,3,6,7) **(B)** Y = Σ (2,3,7)
(C) Y = Σ (1,2,4,5) **(D)** Y = Σ (2,5,6,7)

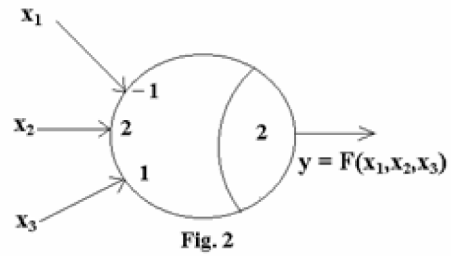

Fig. 2

i. A modulo-P twisted-tail ring counter uses

(A) P binary variable **(B)** 2P binary variable
(C) P/2 binary variable **(D)** None of the above

j. Typical uses of shifters include

(A) Removal of the leading (or trailing) bits of a vector
(B) Performing multiplication or division by a power of two.
(C) Extracting a subvector from a bit-vector
(D) All the above

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Use the tabulation procedure to generate the set of prime implicants and to obtain *all* minimal expressions for the following function:

$f(v,w,x,y)=\sum(1,5,6,12,13,14)+\sum_{\phi}(2,4)$ **(9)**

b. Find whether the function $f(w,x,y,z)=\sum(0,1,3,5,8,10,11,12,13,15)$ is symmetric and if so express the function in symmetric notation. **(7)**

Q.3 a. Explain the following:-

(1) FPGAs
(2) Shift registers
(3) Priority encoder **(9)**

b. Using a ROM, implement a system that converts from BCD to Seven segments. **(7)**

Q.4 a. Implement the following function with NAND gates:-
$f(x, y, z) = \sum (0,6)$ **(6)**

b. Explain features of Computer Aided Design Tools. **(4)**

c. Explain how functional decomposition is done. Give an example. **(6)**

Q.5 a. Explain identification and realization of threshold functions. **(5)**

b. Give an example of data sub system and control sub system. **(7)**

c. Explain explicit sequencing and implicit sequencing used in microinstruction sequencing. **(4)**

Q.6 a. Explain critical race and non-critical race used in asynchronous sequential machines. **(5)**

b. Explain limitations of finite state machines. **(3)**

c. Draw the ASM chart and state diagram for the synchronous circuit, which has enable input E, clock and outputs A, B, C. **(8)**

(i) If E= 1, on every rising edge of the clock code on output A, B, and C changes from 000 → 011 → 101 → 111→ 000 and repeats.
(ii) If E= 0, then the circuit holds present state.

Q.7 a. Write short notes on:- **(8)**
(i) Horizontal and vertical microinstruction format
(ii) Synchronous sequential machine and asynchronous sequential machine

b. Draw the structure of microprogrammed controller and explain its functionality. **(8)**

Q.8 a. Write VHDL code for the following:- **(8)**
(i) 3×8 decoder
(ii) JK flip flop

b. Draw the block diagram of Programmable Sequential Array (PSA) and explain various inputs and outputs. **(4)**

c. Explain minimization of flow tables in synchronous sequential machines. **(4)**

Q.9 a. Design full subtractor using structural modeling, in VHDL. **(6)**

b. Mention various components used in VHDL design. **(4)**

c. Compare behavioural, structural and data flow models used in VHDL. **(6)**