JUNE 2008

Code: AE27 **Subject: DIGITAL HARDWARE DESIGN**

Time: 3 Hours **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. The Mealy circuit output depends

(A) only on the present state of the flip flop
(B) only on the next state of the flip flop
(C) on both present state and the next state of the flip flop
(D) None

b. In _____type of register ,we have access only to left and right most flip-flops

(A) serial in serial out **(B)** serial in parallel out
(C) Parallel in serial out **(D)** parallel in parallel out

c. The output frequency of a MOD-16 counter, clocked by a 10 KHz signal is

(A) 2.5KHz **(B)** 6.25 KHz
(C) 625 Hz **(D)** 10KHz

d. The minimum number of NAND gates required to implement the function
$f = (\bar{x} + \bar{y})(z + w)$

(A) 3 **(B)** 4
(C) 5 **(D)** 6

e. Which of the following statements are true with respect to DEMUX

(A) Uses SELECT inputs
(B) Only one set of outputs can be activated at a time
(C) Can be used to route an input signal to one of several possible outputs
(D) All of the above

f. In a tabular method, the minimal expression of a function contains _____

(A) Only Prime implicants
(B) Prime implicants and Essential Prime implicants
(C) Only Essential Prime implicants
(D) All variables

g. In VHDL, with respect to package body which of the following statement is not true

(A) It is used to store definitions of functions and procedures that are declared in corresponding package declaration.
(B) Package body is always associated with package declaration.
(C) Package declaration can have multiple package bodies associated with it
(D) Package body is not necessary if the corresponding package declaration has no function, procedure or no deferred constant declarations.

h. Full subtractor can be realized by using

(A) One half-subtractor and one OR gate.
(B) Two half-subtractors and one OR gate.
(C) One half- subtractor and one AND gate.
(D) Two half- subtractors and one AND gate.

i. Which of the following is an example of sequential circuit

(A) Parallel adder **(B)** Serial adder
(C) BCD adder **(D)** Look ahead adder

j. The PLA program table contains_____.

(A) Outputs and number of states
(B) Next states and control outputs
(C) Present state and control outputs
(D) Inputs, outputs and product terms

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Simplify the following using K-map

(i) $f(a,b,c,d,e) = \sum m(0,2,4,6,9,11,13,15,17,21,25,27,29,31)$

(ii) $f(a,b,c,d,e) = \sum m(13,15,17,18,19,20,21,23,25,27,29,31) + \sum d(1,2,12,24)$ **(4x2)**

b. Solve by tabulation method-

$$f(a,b,c,d) = \sum m(1,2,3,9,12,13,14,) + \sum d(0,7,10)$$ **(4)**

c. Simplify the following Boolean function using only NOR gates

$$Y = (\bar{A} + B + C)\ (A + B)\ D$$ **(4)**

Q.3 a. What are combinational circuits, list any four combinational circuits? **(2)**

b. Draw the truth table for full adder and construct the full adder circuit using (i) two half adder circuits , (ii) XOR -NAND gates

With proper logic diagram represent the construction of a 4-bit parallel subtractor using full adders. **(8)**

c. Design a combinational circuit with four inputs and two outputs. One of the outputs is high when majority of inputs are high. Second output is high only when all inputs are of same type. **(6)**

Q.4 a. Explain with proper example how a priority encoder works? **(4)**

b. Implement 16:1 multiplexer using 8:1 multiplexer. **(4)**

b. Draw Mealy machine state-diagram for a sequence (0101) detector and design logic diagram. **(8)**

Q.5 a. By examining the linear inequalities ,determine which of the following function is threshold function and find its corresponding weight threshold vector.

(i) $f_1(x_1,x_2,x_3) = \sum m(1,2,3,7)$

(ii) $f_2(x_1,x_2,x_3) = \sum m(0,2,4,5,6)$ **(4x2)**

b. State the capabilities and limitations of threshold logic. **(4)**

c. Write short note on ASM chart. **(4)**

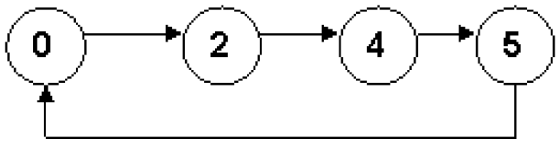
Q.6 a. Compare - PROM, PLA and PAL. **(8)**

b. Write a VHDL program for a 4x1 multiplexer using structural, data-flow and mixed style. **(8)**

Q.7 a. Compare and contrast asynchronous and synchronous sequential circuits. **(4)**

b. Write a brief note on a micro-programmed controller. **(4)**

c. Design a sequence generator using T-flip flops for the given sequence. Check for lock-out condition.



(8)

Q.8 a. What are the four object classes that can be declared in VHDL? **(4)**

b. Write VHDL code for 1 bit full adder in mixed style of modeling? **(6)**

c. Discuss the 'data-paths' as the component of data subsystem. **(4)**

d. List any three benefits of using a digital system. **(2)**

Q.9 a. Write short notes on -

(i) Digital design using CAD-tools
(ii) FPGA
(iii) Static and dynamic hazards
(iv) Capability and features of VHDL **(10)**

b. Explain the state-assignment in asynchronous sequential circuits when two or more secondary variables are required to change their values simultaneously. **(6)**