Code: A-27 **Subject: DIGITAL HARDWARE DESIGN**

December 2005

Time: 3 Hours

Max. Marks: 100

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: **(2x10)**

a. The threshold element shown in Fig. 1 realises the switching function

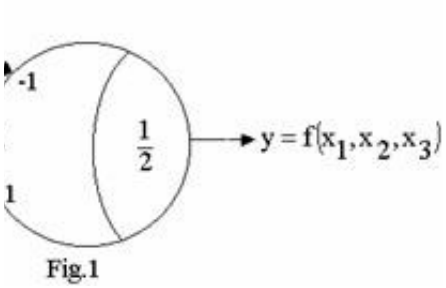

Fig.1

(A) $y = \sum (1, 2, 3, 6, 7)$.

(B) $y = \sum (4, 5, 7)$.

(C) $y = \sum (1, 2, 4, 5)$.

(D) $y = \sum (2, 5, 6, 7)$.

b. A pulse mode asynchronous circuit is having 2 levels of excitation logic with propagation delay of 5 ns each and a latch with delay of 10 ns. Minimum input pulse width required for the circuit is

(A) 5 ns **(B)** 10 ns
(C) 15 ns **(D)** 20 ns

c. A mealy machine is

(A) level input pulse output machine.
(B) pulse input level output machine.
(C) pulse input pulse output machine.
(D) level input level output machine.

d. In Moore machine, output is a function of

(A) present state and external inputs.
(B) only present state.
(C) only external inputs.
(D) neither present state nor external inputs.

e. Which of the following is a unate function

(A) $x'z + x'y + w'z$
(B) $x'y + xy' + x'y'$
(C) $x'z + xz + yz'$
(D) $xz + yz' + xy'$

f. Fig. 2 is block diagram of a multiplier that multiplies two-bit binary numbers. How many output variables (x) are needed for it

(A) 2
(B) 4
(C) 6
(D) 8

g. The circuit shown in Fi

(A) 2-bit up down cc
(B) 4-bit up down cc
(C) 4-bit ring counter
(D) 4-bit Johnson cou

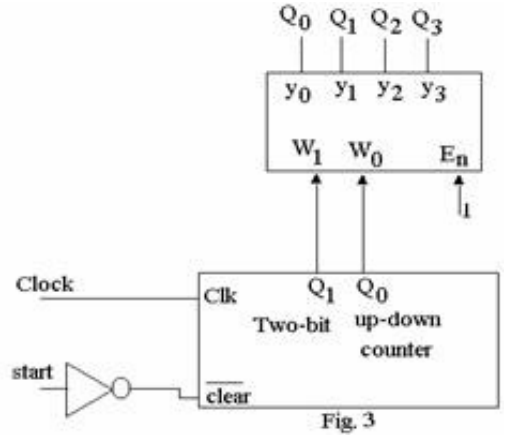

Fig. 3

h. Time t_1 and t_2 shown in Fig.4 respectively represent

(A) set up and hold time.
(B) hold and set up time.
(C) rise and fall time.
(D) fall and rise time.

i. Canonical sum of pr

(A) $pqs + pqs' + p$

(C) $pq's + pqs' + p$

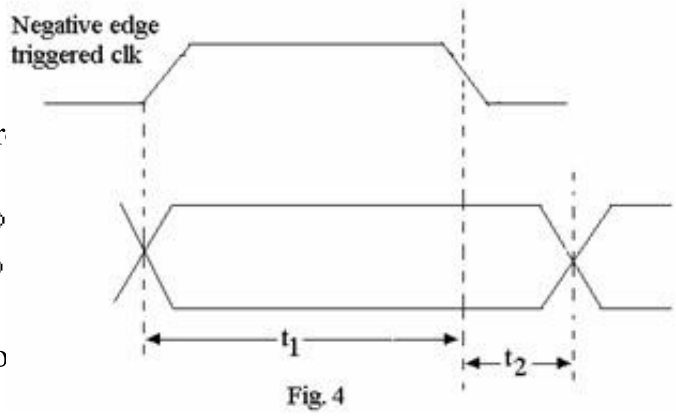

Fig. 4

j. An n-bit Johnson co

(A) $n/2$.

(B) 2 n.

(C) 4 n.

(D) n.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Derive a minimum-cost realisation of a four-variable function that is equal to 1 if exactly two or exactly three of its variables are equal to 1, otherwise it is equal to 0. **(6)**

b. A circuit with two outputs has to implement the following functions:

$f(x_1, x_2, x_3, x_4) = \sum m(0, 2, 4, 6, 7, 9) + d(10, 11)$

$g(x_1, x_2, x_3, x_4) = \sum m(2, 4, 9, 10, 15) + d(0, 13, 14)$

Design a minimum-cost circuit to complement the above function. Compare its cost with combined costs of two circuits that implement the functions f and g separately. Assume that inputs are available in both uncomplemented and complemented form. **(10)**

Q.3 a. The function $f(x_1, x_2, x_3, x_4, x_5) = \sum m(4, 7, 8, 11, 13, 14, 23, 27, 28, 29, 30)$ can be decomposed to the form $F(\Phi(x_1, x_4, x_5), x_2, x_3)$. Determine the function F and Φ . **(6)**

b. Design a single digit BCD adder using an EPROM. Determine the minimum size (mxn bits) of the EPROM. **(10)**

Q.4 a. Explain with the help of a suitable logic diagram the differences between a registered PAL and a GAL. **(6)**

b. Write a VHDL program for a 4×1 multiplexer. **(4)**

c. Write a VHDL program for a 4 bit shift register. **(6)**

Q.5 The output z of a fundamental, two-input sequential circuit changes from 0 to 1 only when x_2

changes from 0 to 1 while $x_1 = 1$. Further, the output changes from 1 to 0 only when x_1 changes from 1 to 0 while x_2=0.

(i) Find a minimum row reduced flow table. **(8)**

(ii) Show a valid assignment and write a set of hazard free excitation and output equations. **(8)**

Q.6 a. Reduce the state table given below using equivalence class state reduction technique. **(8)**

Present State (PS)	Next State (NS), Output (Z)	
	x=0	x=1
s_0	s_3,0	s_1,0
s_1	s_4,0	s_0,1
s_2	s_6,0	s_5,1
s_3	s_0,1	s_3 0
s_4	s_0,1	s_3 0
s_5	s_2,0	s_1 0
s_6	s_0,1	s_4 0

b. Construct a Mealy state diagram that detects a serial input sequence of 10110. Overlapping of the patterns is possible. When the input pattern is detected, it causes output z to be asserted high. First write the flow table and then reduce it. **(8)**

Q.7 a. Find the reduced state table for the machine M given below: **(8)**

PS	NS, Z_1			
	xy=00	xy=01	xy=10	xy=11
A	A, -	C, 1	E, 1	B, 1
B	E, 0	C, -	-, -	-, -
C	F, 0	F, 1	E, 0	-, -
D	-, -	E, 0	A, -	-, -
E	-, -	-, -	A, 0	D, 1
F	C, 0	-, -	B, 0	C, 1

Machine M

b. What is maximal compatibility? What is the difference between compatible states and maximal compatibility? **(8)**

Q.8 a. For the two given Machines M_1 and M_2, find a bigger machine M which is a serial combination

of M_1 and M_2. **(8)**

PS	NS,Z	
	x=0	x=1
A	B, 0	C, 0
B	A, 1	C, 0
C	B, 1	A, 0

Machine M1

PS	NS,Z	
	y=0	y=1
a	a, 0	b, 1
b	b, 1	a, 1

Machine M2

b. Find the state assignment, by choosing self dependent subset, for the machine given below: **(8)**

PS	NS		Z
	x=0	x=1	
A	E	B	1
B	E	A	0
C	D	A	0
D	C	F	1
E	F	C	0
F	E	C	0

Q.9 a. Write ASM chart for a machine which scans a 3 bit word and produces an output z_2 when last two bits in consecutive 3 bit word are ones and second output z_1 which identifies the start of each 3-bit word. Implement the machine using multiplexers. **(6)**

b. Explain the role of CAD Tools in digital system design. **(6)**

c. Write a brief note on a micro-programmed controller. **(4)**