CE1-R3: ADVANCED COMPUTER ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Give at least four differences between scalar and vector instructions.

b) Give difference between PCI, USB and SCSI Bus Systems.

c) Define grain size. Give an example for fine, medium and coarse grain.

d) Suggest some scheme to replace the memory values in cache when cache miss occurs and it is full.

e) What kind of instruction may cause problem with instruction prefetch?

f) Define diameter with respect to static networks.

g) Briefly explain data flow architecture.

(7×4)

2.

a) Explain with an example the Cache-Coherency. How does two level cache increase performance? Derive the formula for average access time in a three level cache?

b) Describe briefly the dual bus design for shared memory multiprocessors with special emphasis on clustered architecture.

(10+8)

3.

a) Discuss in detail various interconnect architecture for MIMD computers.

b) How will the following code be vectorized? Explain

```
for (i=o; i<1024; i++)
      { if(x[i] > 0)
            y[i] = z[i];
            else
            w[i] = w[i-1];
      }
```

(9+9)

4. Describe the following terminology associated with multiprocessors.

a) Mutual exclusion

b) Critical section

c) Hardware lock

d) Semaphore.

(4×4.5)

5.

a) Briefly explain speed up in a pipeline with K-stages.

b) Explain data dependency among pipeline stages.

(10+8)

6.

a) What is the difference between superscalar and super pipelined process?

b) What are the limitations of instruction level parallelism that affect superscalar performance?

(9+9)

7.

a) Explain branch handling strategies for a pipelined processor under hierarchical memory system.

b) What is a stride? How does it affect the design of vector memory? Give an example.

(10+8)