CE1-R3: ADVANCED COMPUTER ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR from questions 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Describe briefly SIMD machine model.
b) What are the limitations of instruction-level parallelism? Explain briefly.
c) Explain the cluster model of memory organisation, with the help of suitable diagrams.
d) Explain briefly how RISC architecture attempts to reduce execution time.
e) Differentiate between Loosely Coupled System and Tightly Coupled System?
f) Explain the crossbar network.
g) How is performance of the processors improved by using the superscalar architecture?

(7x4)

2.

a) Describe instruction pipelines for CISC scalar processors with respect to instruction prefetching, data forwarding and hazard avoidance.
b) How can the penalties of branches and jumps be reduced in pipeline performance?

(10+8)

3.

a) What are various three types of dependencies? Describe each briefly with an example.
b) I/O bus standard defines how to connect computer system and device. What is the mechanism for the same?

(12+6)

4.

a) What are the various techniques for reducing cache miss penalty?
b) Why do we need virtual memory among many processes? Explain briefly.

(12+6)

5.

a) In program parallelism, what are different issues of parallelism?
b) What do you mean by wormhole routing? Where do we need it? Explain.
c) In vector processing, how do we handle the situation when vector length of the program is not exactly 64?

(6+6+6)

6.

a) How vector processor instructions have helped to improve parallelism? What are the primary components of instruction format of a typical vector processor?
b) What is pipeline bubble? Explain with an example.

(12+6)

7.

a) Write down on $O(n^2)$ algorithm for SIMD matrix multiplication. Establish the correctness of the complexity.
b) Describe the procedure of mapping DGs and SFGs to systolic arrays.

(10+8)