JUNE 2008

Code: AE13 **Subject: COMPUTER ENGINEERING**
Time: 3 Hours **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or best alternative in the following: (2x10)

a. When several computations are performed concurrently in a computer it is known as

(A) Pipelined computers **(B)** Array processors
(C) Multiprocessor systems **(D)** Parallel processing

b. The BCD equivalent of 84 is

(A) 0100 1000 **(B)** 1000 0100
(C) 1100 0110 **(D)** 1100 0100

c. If the 8085 microprocessor instruction MOV C,B takes 5T states to execute and if the system clock frequency is 750kHz, calculate the time the instruction takes to execute

(A) 7.77 μsec **(B)** 5.55 μsec
(C) 6.66 μsec **(D)** 4.44 μsec

d. A certain SRAM stores 1 Mb. If this chip is organized as X8, it stores the following number of bytes.

(A) 128 K **(B)** 256 K
(C) 64 K **(D)** 1280 K

e. Fusible-link PROM's are said to be

(A) Infinite-time programmable **(B)** Electrically many time programmable
(C) Not at all programmable **(D)** one-time prorammable

f. If the address sent by the CPU matches with the address present in the cache then it is said the following as occurred.

(A) Miss **(B)** Hit
(C) Match **(D)** Shot

g. If the baud rate is 440, then in 64X mode the $\overline{\tau \times c}$ is equal to

(A) 28.16 kHz **(B)** 56.14 kHz
(C) 16.82 kHz **(D)** 32.82 kHz

h. What 386 operating mode allows the processor to run multiple real mode programs simultaneously

(A) Protected mode **(B)** Virtual 8086 mode
(C) Safe mode **(D)** Physical mode

i. Programming an EISA interrupt using the following triggering allows that interrupt to be shared by several devices

(A) Edge **(B)** Level
(C) Low **(D)** High

j. The number of devices that can be connected when 8259 are cascaded

(A) 8 **(B)** 64
(C) 16 **(D)** 32

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. What is an Array processor? Describe its operating principle. Can an array processor operate independently? **(6)**

b. What are RISC and CISC processors? What is the impact of computers on society? **(6)**

c. 01H, 36H, E5H are received over a serial data line and if these bytes are encoded using even parity, in which of these bytes there is error, if any. **(4)**

Q.3 a. Explain the Edit, Assemble, Test and debug cycle of a program in source-code form to be executed by a computer. **(6)**

b. Give the major functions of UNIX kernel and the important features of UNIX shell. **(2+3)**

c. Give the memory map of an 80x86 computer running MS-DOS. **(5)**

Q.4 a. Draw and explain the 8085 timing diagram of the Memory Read Cycle? **(8)**

b. Explain Immediate, Register, Register Indirect, Based Indexed addressing modes of 8086 Microprocessor with an example for each addressing mode. **(8)**

Q.5 a. Explain about (i) Static RAM (ii) Dynamic RAM (iii) SIMMs (iv) DIMMs (v) RIMMs **(8)**

b. (i) How many 128 x 8 RAM chips are needed to produce a memory capacity of 2048 bytes?
(ii) How many lines of address bus must be used to access 2048 bytes of RAM? How many of these lines are common to all chips?
(iii) How many lines must be decoded for chip select? Specify the size of the decoder.
(3+3+2)

Q.6 a. Explain the two different modes of transferring data from the peripheral to system memory under the DMA controller. **(8)**

b. Write an 8085 initialization program to transfer 256 bytes of data from a peripheral (floppy disk) to memory, starting at 2050H. After the transfer, the DMA operation should be terminated. **(8)**

Q.7 a. Explain the mode word, command word, status word format of 8251 (USART). **(8)**

b. Explain the control word of 8255A and write an 8085 microprocessor assembly languages program to read the DIP switches and display the reading from port B at port A and from port C_L at port C_V (Assume your own address decoding logic). **(8)**

Q.8 a. Explain in brief about
(i) MIPS microprocessors
(ii) CYRIX microprocessor
(iii) AMD processor
(iv) SUN's Ultra SPARC **(8)**

b. Explain the 80386 protected mode and explain how physical addresses are computed in this mode. **(8)**

Q.9 a. Show how the 8255A PPI chip can be interfaced to the I/O bus of the PC/XT so that the chip is mapped to ports 3FC–3FFH. What are the commands to program the chip for mode 0 operation with ports A and B operating as input ports and port C as an output port? **(8)**

b. Describe plug-and-play ISA and explain how plug and play works? **(4)**

c. Calculate the time for one PC bus cycle, assuming a 4.77 MHz clock frequency. What is the data transfer rate for this bus? **(4)**