SATHYABAMA UNIVERSITY

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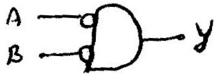
Course & Branch :B.E - EEE
Title of the Paper :Digital Systems   Max. Marks :80
Sub. Code :6C0038   Time : 3 Hours
Date :04/05/2010   Session :FN

PART - A   (10 x 2 = 20)
Answer ALL the Questions

1. State De-Morgan's theorem.

2. Convert the gray code number 11011 to gray.

3. Mention the drawbacks of K-map method.

4. Define priority encoder.

5. Find the relation between the inputs and output shown in figure.

6. Write the truth table of 4:1 Mux.

7. How does a J-K flip flop differ from SR flip flop?

8. What is race around condition?

9. Which memory is called volatile? Why?

10. Define Noise margin.

PART – B   (5 x 12 = 60)

Answer All the Questions

11. (a) Prove the following using De-Morgan's theorem.
$(A+B) \cdot (C+D) = ((A+B)'+(C+D)')'$
(b) Represent the decimal number 396 and 4096 in
(i) Binary code
(ii) BCD code
(iii) Excess-3 code
(iv) Hex code
(v) Octal code

(or)

12. (a) State and prove the consensus.
(b) Illustrate the rules for binary addition and subtraction using 2's complement arithmetic. Give example.

13. using a Karnaugh map determine the MSP and MPS forms of the switching function
$F = \Sigma(0, 1, 2, 4, 6, 8, 9, 11, 14, 15)$

(or)

14. Implement the Boolean expression
$F_1 = x'z + y'z'$
$F_2 = x'y + x'z.xy'$
Using a PLA.

15. Implement the following with a multiplexer.
$F(A,B,C,D) = \Sigma(0,1,3,4,5,6,8,9,10,11,12,13,14,15)$

(or)

16. Design a BCD adder to add two BCD digits.

17. (a) Derive the characteristic equation of T flip flop.
(b) Explain in detail about Universal shift register.

(or)

18. Design a synchronous mod-8 down counter.

19. Describe the RAM organization.

<div align="center">(or)</div>

20. (a) Explain the operation of 3 input TTL NAND gate with required diagram and truth table.

    (b) Write short notes on RTL.