DiplETE – CS (NEW SCHEME) – Code: DC57

Subject: COMPUTER ORGANIZATION

Time: 3 Hours   Max. Marks: 100

DECEMBER 2009

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1   Choose the correct or the best alternative in the following: (2×10)

a. The basic performance equation for a computer is

(A) $T = \dfrac{N \times S}{R}$ (B) $T = \dfrac{N \times R}{S}$

(C) $N = \dfrac{S \times R}{T}$ (D) $T = \dfrac{S \times R}{N}$

b. SPEC corresponds to

   (A) System Performance Evaluation Corporation
   (B) Signed Processor Evaluation Condition
   (C) Saturated Processor Evaluation Condition
   (D) Signal performance Evaluation Condition

c. First generation computer (Von Neuman Machine)

   (A) ENIAC   (B) EDVAC
   (C) IAS Processor   (D) Parallel Processor

d. The number 100110_2 is numerically equivalent to

   (A) 26_{10} (B) 36_{10}
   (C) 46_8 (D) $2A2_{16}$

e. The first byte of a 3 byte instruction will always have

   (A) the address of memory   (B) an operand or address
   (C) opcode   (D) anyone of the above

f. In 4 bit carry look ahead adder, the addition process requires only

   (A) 4 gates delay   (B) 3 gates delay
   (C) $1 \times \theta V$ gate delay   (D) 2 gates delay

g. The 2114 memory IC is $1K \times 4$ state RAM which means it has _____ memory locations with _____ data bits at each location

(A) 1024, 4   **(B)** 41, 1024

(C) $10^{11}, 2$ **(D)** $10^{12}, 2$

h. The data bus width of a memory of size 2048×8 is

(A) 16   **(B)** 32

(C) 12   **(D)** 16

i. A Charge Coupled Device CCD is

(A) magnetic device   **(B)** bipolar SC device

(C) MOS device   **(D)** none of the above

j. The maximum positive and negative numbers which can be represented in 1's complement form using n bits are

(A) $+\left(2^{n-1}-1\right), -\left(2^{n-1}-1\right)$ **(B)** $-0, \left(2^{n-1}-1\right)$

(C) $+0, -\left(2^{n-1}-1\right)$ **(D)** $2^{n-1}, -\left(2^{n-1}+1\right)$

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2   a.   Explain in brief the evolution of computer systems.   **(8)**

      b.   Write a short note on multi computers and multiprocessors.   **(4+4)**

Q.3   a.   Explain the following with examples:
           (i)   Byte addressability
           (ii)   Big Endian assignment
           (iii)   Little Endian assignment   **(2+3+3)**

      b.   Both of the following statements cause the value 300 to be stored in location 1000, but at different times
         ORIGIN 1000
         DATAWORD 300
         And
         MOVE #300, 1000

         Explain the difference.   **(8)**

Q.4   a.   Explain any two methods of handling multiple I/O devices.   **(4+4)**

      b.   The address bus of a computer has 16 address lines, $A_{15} - 0$. If the address assigned to one device is $7CA4_H$ and the address decoder for that device ignores lines A_8 and A_9. What are all the addresses to which this device will respond?   **(8)**

Q.5   a.   Explain any two cache mapping functions.   **(8)**

      b.   Draw the disk controller interface connection and explain the major functions of disk controller.   **(8)**

Q.6   a.   A block set-associative cache consists of a total of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks each consisting of 128 words
(i)   How many bits are there in a main memory address?
(ii) How many bits are there in each of the TAG, SET and WORD fields?   **(4+4)**

   b.   Represent the following pairs of decimal numbers in 2's complement form of size 8 bits. Add each pair and obtain the results along with the sign, carry and overflow flags that will be generated as a result of this addition. Comment on the results.
(i)   35 & -120   (ii) -35 & -120   **(4+4)**

Q.7   a.   Why is wait-for-memory-function-completed step needed when reading from or writing to the memory? Explain.
(4)

   b.   Compare Microprogrammed control vs Hardwired control.   **(12)**

Q.8   a.   Define the IEEE standard single precision floating point format and obtain the range of numbers that can be represented in that format.   **(8)**

   b.   Workout in Hexadecimal the single precision IEEE representation for -12.5_{10} .   **(8)**
Q.9   Write short notes on:

(i)   Carry look ahead addition   **(8)**

(ii) Booth's Algorithm for the signed 2's complement numbers
A = 110011 (multiplicand)
B = 101100 (multiplier)   **(8)**