C13-R3: DIGITAL SYSTEM DESIGN

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Given $(292)_{10} = (1204)_{b,}$
Determine b.

b) What do you mean by Fan-out and Fan-in in context with TTL integrated circuit?

c) What is a Karnaugh map? Why cyclic codes are used in listing the combinations as column and row heading of a Karnaugh Map?

d) Connect a Multiplexer with demultiplexer so that parallel input/output is produced by a serial interconnection.

e) The content of a 4-bit register is initially 1101. The register is shifted six times to the right with the serial input 101011. What is the content of the register after each shift?

f) What is an information processing machine? Consider a Finite state machine that accepts a sequence of positive integers between 0 to 1 and produces at any instant the largest integer that the machine has so far received as output. What is the output of the machine with input sequence 3,4,9,7,5,7,3,4,? What is the number of states of the FSM?

g) Find the number of 1's in a byte using ROM. What is the time and space complexity of the design?

(7x4)

2.

a) Describe the functioning of PLA with a block diagram.

b) Write assembly language programs with usual opcodes (like LD, ST, M, A) for the expression X= A*B+C*D in zero, one, two and three address machines.

(4+14)

3.

a) What are differences between MOS and junction transistor?

b) Describe enhancement and depletion mode devices. Show their role in MOS circuit design.

(8+10)

4.

a) When a set of gates is said to be to be functionally complete?

b) Design a three input, one output minimal two-level gate combinational network that has a logic-1 output when majority of its inputs are logic-1 and has a logic-0 output when the majority of its inputs are logic 0.

c) Why well formed combinational circuits are acyclic?

(6+10+2)

5.

a) Comment on hardware description languages highlighting its positive and negative sides.

b) Give VHDL description of Half Adder.

(8+10)

6.

a) What is the main difference between Random Access Memory (RAM) and Read Only Memory (ROM)?

b) 7489 is a 16*4 RAM chip with chip enable and open collector output. Design 32*4 RAM unit and 16*8 RAM unit using two such Units. Only functional diagram is required.

(4+14)

7.

a) What is key Bounce and Debounce?

b) Design a Hardware circuit using NAND latch to eliminate Key Bounce and Debounce.

(6+12)