C13-R3: DIGITAL SYSTEM DESIGN

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Obtain a clocked T flip-flop using a clocked D flip-flop as basic unit.

b) Prove that NAND and NOR gates are universal logic gates.

c) Realize the following function using an 8 X 1 multiplexer.
$F = \Sigma(0,1,10,11,12,13,14,15)$

d) In the clocked SR latch, the simultaneous conditions S = R = 1 results in an uncertain state. A variation on the SR latch is the set-dominate latch. For this latch, simultaneously high inputs result in setting the latch, that is setting Q = 1. Construct a transition table for the SD latch. From this, determine an expression for the next state.

e) Draw a synchronous sequential circuit with a single input line x and a single output line z, so as to produce an output z = 1 whenever an input symbol completes as sequence of 4 identical input bits; the output is to be 0 otherwise. Also write its Boolean function expression.

f) Write the description of a full adder in VHDL.

g) What size of the ROM would take to implement:
   i) A BCD adder/Subtractor with a control input to select between the addition and subtraction.
   ii) A binary multiplier that multiplies two 4–bit numbers.
   iii) Dual 4–line to 1-line multiplexers with common selection inputs.
   iv) A BCD to Exess-3 code converter.

(7x4)

2.

a) Use 2's complement and the 1'st complement method to perform M–N with the given binary numbers:
   i) M = 1010100 and N = 1000100
   ii) M = 1000100 and N = 1010100

b) Simplify the following Boolean function to a minimum number of literals using the axioms of Boolean algebra.
   X'Y'Z + X'YZ + X'Y

c) Express the Boolean function F = XY + X'Z in a product of maxterm form.

d) Obtain a binary code to represent all base-6 digits so that the 5's complement is obtain by replacing 1's by 0's and 0's by 1's in the bits of the code.

e) A majority gate is a digital circuit whose output is equal to 1 if the majority of the inputs are 1's. The output is 0 otherwise. By means of a truth table, find the Boolean function implemented by a 3-input majority gate. Simplify the function.

(8+2+2+2+4)

3.

a) The following Boolean expression:
   BE+B'DE'
   Is a simplified version of the expression?
   A'BE+BCDE+BC'DE+A'B'DE'+B'C'DE'
   Are there any don't –care conditions? If so, what are they?

b) Implement the following function with either NAND or NOR gates. Use only four gates. Only the normal inputs are available.
F = W'XZ + W'YZ + X'YZ' + WXY'Z
D = WYZ (Where D stands for the don't care condition)

c) Implement the four Boolean functions listed using three half-adder circuits.
D = A (EX-OR) B (EX-OR) C
E = A'BC + AB'C
F = ABC' + (A'+B') C
G = ABC

(6+6+6)

4.

a) A combinational circuit is defined by the functions:
$F_1 (A, B, C) = \sum (3, 5, 6, 7)$
$F_2 (A, B, C) = \sum (0, 2, 4, 7)$
Implement the circuit with PLA having three inputs, four product terms and two outputs.

b) Design a combinational circuit using ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number.

c) Using 4 exclusive – OR gates and 4 – bit full adder MSI circuit, Construct a 4-bit parallel adder/subtractor. Use an input select variable V so that when V = 0, the circuit adds and when V = 1, the circuit subtracts.

d) Implement the following function with a 8 X 1 multiplexer:
$F (A, B, C, D) = \sum (0, 1, 3, 4, 8, 9, 15)$

(5+5+5+3)

5.

a) Design a counter that has a repeated sequence of six states as listed below:
000,001,010,100,101,110

b) Design a sequential circuit with JK flips – flops to satisfy the following state equations:
A (t+1) = A'B'CD + A'B'C + ACD + AC'D'
B (t+1) = A'C + CD' + A'BC'
C (t+1) = B
D (t+1) = D'

c) Consider a JK flip–flop, i.e. a JK flip-flop with an inverter between external input K' and internal input K.
i) Obtain the flip-flop characteristic table.
ii) Obtain the characteristic equation.
iii) Show that tying the two external inputs together forms a D flip-flop.

d) Design the sequential circuit whose state table is given below using a 2-bit register and combinational gates.

Present State		**Input**	**Next state**	
A	**B**	**X**	**A**	**B**
0	0	0	0	0
0	0	1	0	1
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	1	1
1	1	0	1	0
1	1	1	0	1

(3+5+6+4)

6.

a) A synchronous sequential circuit having a single input x and a single output z is to be designed. The output z is to become 1 upon completion of the input sequence 0101, whether it forms part of an overlapping string (such as 00010101) or not.
   i) Construct a state diagram and a state table.
   ii) Construct an appropriate state assignment map.
   iii) Assume the use of JK flip-flops and construct a transition table.
   iv) Construct excitation and output map.
   v) Draw the diagram of the resulting circuit.

b) Write the VHDL description of a 4-bit serial adder. Assume one operand is stored in a shift register and the result is stored in same shift register. Write the description hierarchically by creating a shift register module and as adder module and including them in the serial adder module.

(10+8)

7.

a) Determine the states of the data-path registers at each step of the multiplication procedure for a multiplicand of 0101 and a multiplier of 1101.

b) Write the RTL notation of the micro-operations for the store and NAND operations the simple CPU.

c) Design the control and data path units of a processor that accumulates four 8-bits numbers provided sequentially. In four consecutive clock cycles, four 8-bit numbers are provided at the inputs and the processor should accumulate their values in a register. The processor automatically starts again after the last of the four inputs is received. Sketch a block diagram of the data path unit.

(5+5+8)