DipIETE – ET (NEW SCHEME) – Code: DE56

Subject: ANALOG ELECTRONICS

Time: 3 Hours **JUNE 2009** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. Small scale integration (SSI) chip contains approximately

(A) 10 transistors **(B)** 100 transistors
(C) 1000 transistors **(D)** 10000 transistors

b. The purpose of using emitter bypass capacitor in a voltage amplifier is to

(A) avoid ac degeneration **(B)** increase input impedance
(C) decrease input impedance **(D)** decrease output impedance

c. The voltage gain of common collector amplifier is

(A) < 1 **(B)** > 1
(C) > 10 **(D)** < 10

d. FET is a

(A) current operated device **(B)** power operated device
(C) resistance operated device **(D)** voltage operated device

e. The maximum power conversion efficiency of Class A transformer coupled power amplifier is

(A) 25% **(B)** 75%
(C) 50% **(D)** 78.5%

f. The material used in light emitting diode is

(A) Silicon **(B)** Germanium
(C) Glass **(D)** Gallium arsenide

g. The slew rate of an opamp with an internal capacitor of 30 pF and maximum internal capacitor charging current of 15 μA is

(A) $1V/\mu s$ **(B)** $5V/\mu s$
(C) $0.5V/\mu s$ **(D)** $0.1V/\mu s$

h. Commonly used audio power amplifier chip is

(A) $\mu A741$ **(B)** LM 380

(C) 7400 **(D)** 555

i. The input to Astable multivibrator is

(A) sine wave **(B)** square wave
(C) triangular wave **(D)** no input

j. The fastest type of ADC is

(A) counter type **(B)** flash type
(C) dual-slope type **(D)** successive approximation type

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. List the basic processes used in the silicon planar technology and describe photolithography and diffusion processes. **(12)**

b. Write an explanatory note on thin and thick film technology. **(4)**

Q.3 a. Derive expressions for input impedance, output impedance, voltage gain and current gain of CE transistor amplifier with voltage divider bias using *h* model with emitter resistor by passed. **(10)**

b. Calculate Z_i and Z_o for a common collector circuit with the following component values and parameters. $R_1 = 56\,k\Omega$ $R_2 = 39\,k\Omega$ $R_E = 5.6\,k\Omega$ $R_L = 22\,k\Omega$ $r_s = 400\,\Omega$ $h_{ic} = 1k\Omega$ $h_{fc} = 100$. **(6)**

Q.4 a. With neat diagram explain the working of enhancement mode MOSFET. **(10)**

b. A JFET is used in the amplifier circuit shown in Fig.1. Calculate the minimum and maximum voltages produced by a $\pm 75mV$ AC input. Also calculate the circuit voltage gain in each case. Assume $Y_{fs}(min) = 1000\,\mu mho$ and $Y_{fs}(max) = 5000\,\mu mho$. **(6)**

Q.5 a. With a ne

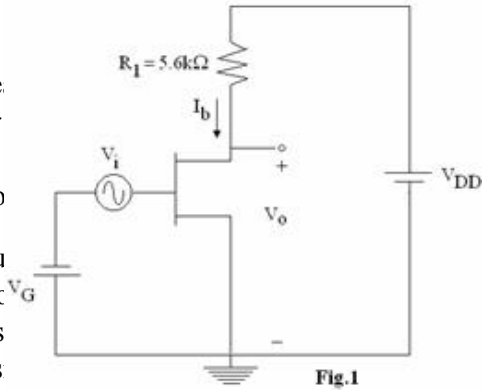

Fig.1

l Class-B power amplifier and obtain an expression for **(10)**

b. Explain the wo **(6)**

Q.6 a. Draw the circu ve expressions for:
(i) closed loc
(ii) input resis
(iii) output res **(10)**

b. For the non-inverting amplifier shown in Fig.2, $R_1 = 1k\Omega$ $R_2 = 10\,k\Omega$.
(i) Calculate the maximum output offset voltage due to $V_{os} = 10\,mV$ and $I_B = 200\,mA$ $I_{os} = 40\,nA$.
(ii) Calculate the value of R_{comp} to reduce the effect of I_B.
(iii) Calculate the maximum output offset voltage if R_{comp} as calculated in the above part (ii) is connected to the circuit. **(6)**

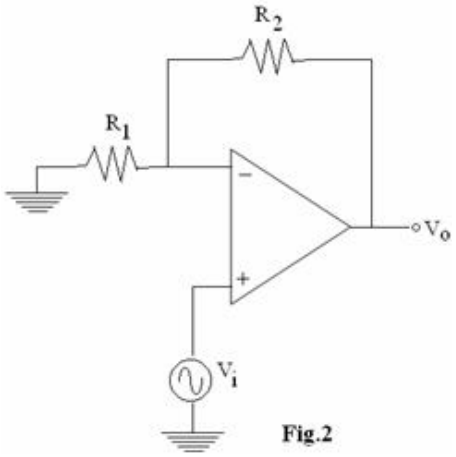

Fig.2

Q.7 a. Draw the circuit of an instrumentation amplifier using three Opamps. Derive expression for output voltage. **(8)**

b. Find the values of R_1 and R_f in the lossy integration circuit using Opamp so that the peak gain is 20 dB. At $\omega = 1000\,rad/sec$ the gain decreases by 3 dB from its peak. Use a capacitance of $0.01\mu F$. **(8)**

Q.8 a. Draw the circuit of a square wave generator using 555 timer. Draw the various waveforms and derive an expression for time period T. **(10)**

b. Design an inverting schmitt trigger circuit having $V_{LT} = 1V$ and $V_{UT} = 2V$. Assume saturated output voltage as $\pm 10V$. Draw the transfer characteristics. **(6)**

Q.9 a. With a diagram and waveforms explain the working of a dual slope ADC. **(10)**

b. Using 7805 voltage regulator, design a current source to deliver 0.2 A current to a 22Ω, 10 W load. Draw the diagram with component values. **(6)**