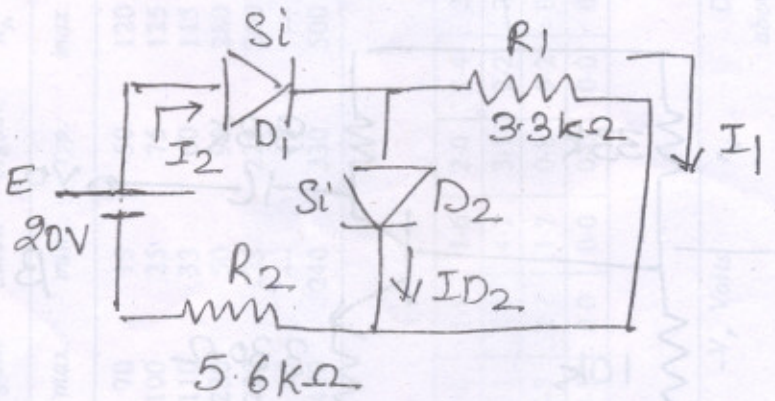
S.E. Electronics SEM III Exam 25 May 2010

Con. 3001-10. Basics of Electronic circuits AN-2479

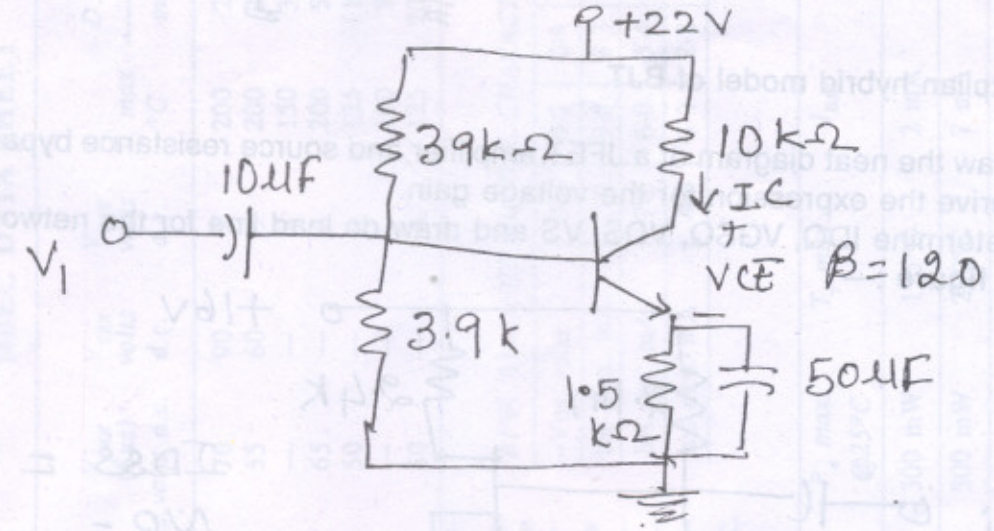
(3 Hours) [Total Marks : 100

N.B. (1) Question No. **1** is **compulsory**.
(2) Answer any **four** out of remaining **six** questions.
(3) Assume any suitable data wherever **required**.

1. (a) Determine the Currents I_1, I_2 and ID_2 for the following network :— 5



(b) Determine the dc bias Voltage VCE and the current IC for the following configuration :— 5



(c) Derive the condition for fero temperature drift biasing of FET. 5
(d) What is the maximum reverse voltage (PIV) across a diode in :— 5
(i) HWR
(ii) FWR with center tapped transformer
(iii) Bridge type rectifier.

2. (a) Design a Single stage BJT CE Amplifier for the following requirements :— 15
Av ≥ 100, Zi > 3K Ω, Vcc = 18 V.
(b) Determine Av, Zi and Zo for designed circuit. 5

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3. (a) Explain the operation of fullwave rectifier and draw the o/p wareform for $V_L$dc and $I_L$dc. 10

(b) Derive an Expression for ripple factor for capacitor filter with center tapped Full wave rectifier. 10

If a circuit of fullwave center tapped rectifier with capacitor filter employs a load $R_L = 100\ \Omega$ and $C = 1050\ \mu F$. Calculate the ripple factor.

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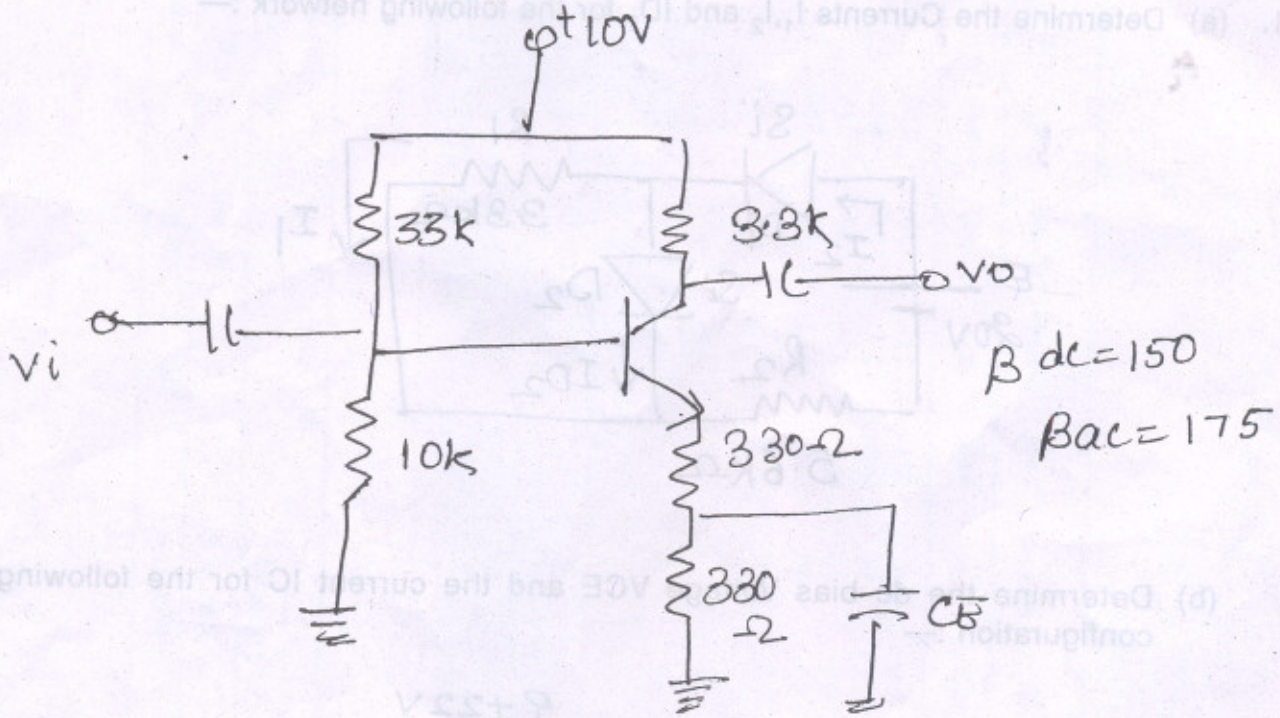
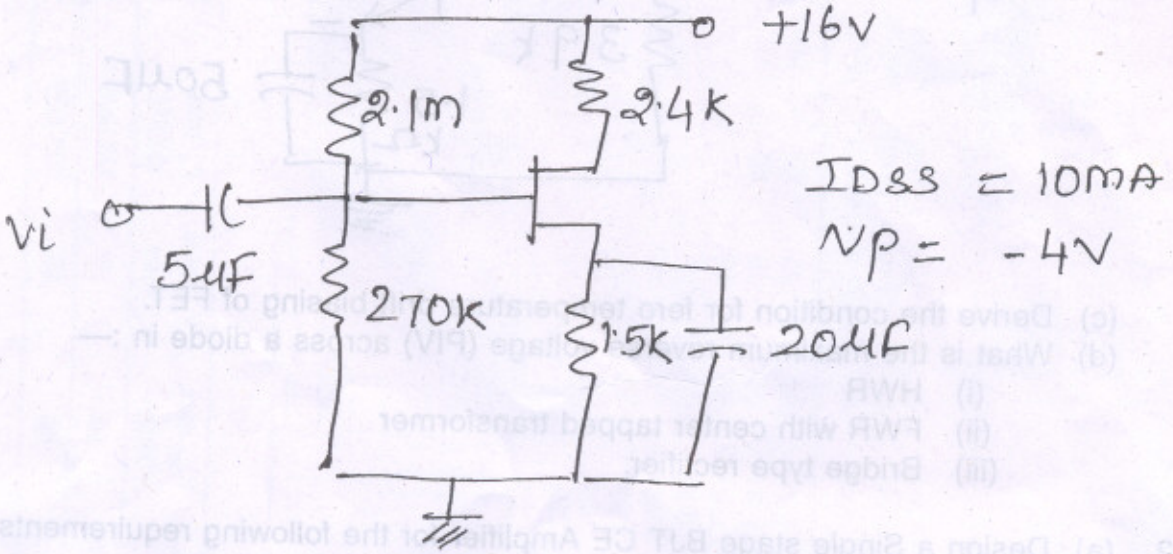
4. (a) For the circuit shown in **figure** determine :— **15**
   (i) Operating point
   (ii) Voltage gain
   (iii) Input impetance
   (iv) What will be Voltage without CE ?
   (v) What will be i/p impetance without CE ?



   (b) Explian hybrid model of BJT. **5**

5. (a) Draw the neat diagram of a JFET amplifier and source resistance bypassed and derive the expression for the voltage gain. **10**
   (b) Determine IDQ, VGSQ, VDS, VS and draw dc load line for the network shown in **figure** :— **10**



6. (a) Explain Construction, Working principle and characteristic of D Mosfet. **10**
   (b) Explain different biasing techniques for E MOSFET. **5**
   (c) Compare MOSFET and FET. **5**

7. Write short notes any **three** of the following :— **20**
   (a) Voltage multiplier

DBEC DATA SHEET

Transistor type	Pdmax @ 25°C Watts	Icmax @ 25°C Amps	$V_{CE}^{(sat)}$ volts d.c.	V_{CBO} volts d.c.	V_{CEO} (Sus) volts d.c.	V_{CER} (Sus) volts d.c.	V_{CEX} volts d.c.	V_{BEO} volts d.c.	T_j max °C	D.C. current gain min	typ.	max.	Small Signal min.	typ.	h_{fe} max.	V_{BE} max.	θ_{fc} °C/W	D a 2 V
2N 3055	115·5	15·0	1·1	100	60	70	90	7	200	20	50	70	15	50	120	1·8	1·5	
ECN 055	50·0	5·0	1·0	60	50	55	60	5	200	25	50	100	25	75	125	1·5	3·5	
ECN 149	30·0	4·0	1·0	50	40	—	—	8	150	30	50	110	33	60	115	1·2	4·0	
ECN 100	5·0	0·7	0·6	70	60	65	—	6	200	50	90	280	50	90	280	0·9	35	
BC147A	0·25	0·1	0·25	50	45	50	—	6	125	115	180	220	125	220	260	0·9	—	
2N 525(PNP)	0·225	0·5	0·25	85	30	—	—	—	100	35	—	65	—	45	—	—	—	
BC147B	0·25	0·1	0·25	50	45	50	—	6	125	200	290	450	240	330	500	0·9	—	

Transistor type	hie	hoe	hre	θja
BC 147A	2·7 K Ω	18μ ℧	1·5 × 10^{-4}	0·4°C/mw
2N 525 (PNP)	1·4 K Ω	25μ ℧	3·2 × 10^{-4}	—
BC 147B	4·5 K Ω	30μ ℧	2 × 10^{-4}	0·4°C/mw
ECN 100	500 Ω	—	——	——
ECN 149	250 Ω	—	——	——
ECN 055	100 Ω	—	——	——
2N 3055	25 Ω	—	——	——

BFW 11—JFET MUTUAL CHARACTERISTICS

–VGS volts	0·0	0·2	0·4	0·6	0·8	1·0	1·2	1·6	2·0	2·4	2·5	3·0	3·5	4·0
IDS max. mA	10	9·0	8·3	7·6	6·8	6·1	5·4	4·2	3·1	2·2	2·0	1·1	0·5	0·0
IDS typ. mA	7·0	6·0	5·4	4·6	4·0	3·3	2·7	1·7	0·8	0·2	0·0	0·0	0·0	0·0
IDS min. mA	4·0	3·0	2·2	1·6	1·0	0·5	0·0	0·0	0·0	0·0	0·0	0·0	0·0	0·0

N-Channel *JFET*

Type	V_{DS} max. Volts	V_{DG} max. Volts	V_{GS} max. Volts	P_d max. @25°C	T_j max.	I_{DSS}	g_{mo} (typical)	$-V_P$ Volts	r_d	Derate above 25°C	θ_{j}
2N3822	50	50	50	300 mW	175°C	2 mA	3000 μ ℧	6	50 KΩ	2 mW/°C	0·59°C
BFW 11 (typical)	30	30	30	300 mW	200°C	7 mA	5600 μ ℧	2·5	50 KΩ	——	0·59° C