S.E. (ETRX) Sem III (R)

Con. 5355-09. (REVISED COURSE) SP–7355

Lib Basic of Electronic Circuits

(3 Hours) [Total Marks : 100

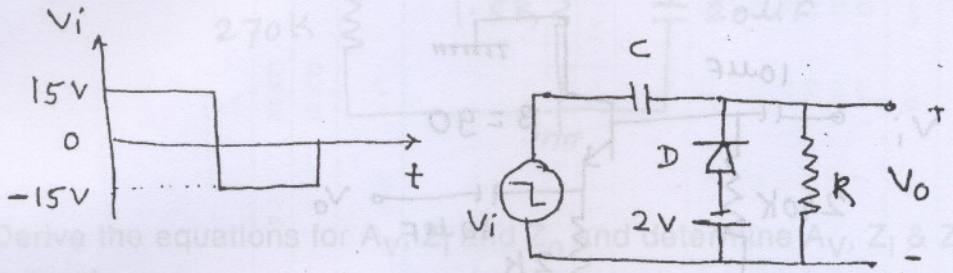
8/12/09

2-30 to 5-30 p.m.

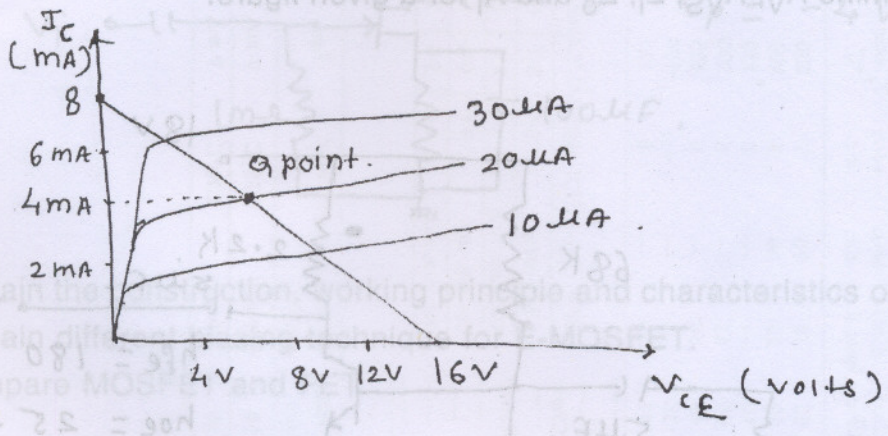
N. B. : (1) Question No. 1 is **compulsory**.
(2) Answer any **four** out of remaining **six** questions.
(3) Assume any **suitable** data, wherever **required**.
(4) Answer to questions should be **grouped** and written **together**.

1. Solve any **four** :— 20

(a) Sketch the o/p waveform for shown figure.



(b) The d.c. load line of fixed bias is shown in figure. Determine the required values of V_{CC}, R_C and R_B for a fixed-bias circuit.



(c) What is maximum reverse voltage (PIV) across a diode in
(i) HWR (ii) a FWR with center tapped transformer (iii) Bridge type rectifier ?

(d) Derive the condition for zero temp. drift biasing of FET.

(e) Which biasing method can not be used for D-MOSFET and Why ?

2. (a) Design single stage BJT CE Amplifier for the following requirements. 15

$A_v \geq 100$, $Z_i > 3K\Omega$, $V_{CC} = 18$ V

(b) Determine A_v, Z_i and Z_o for designed circuit. 5

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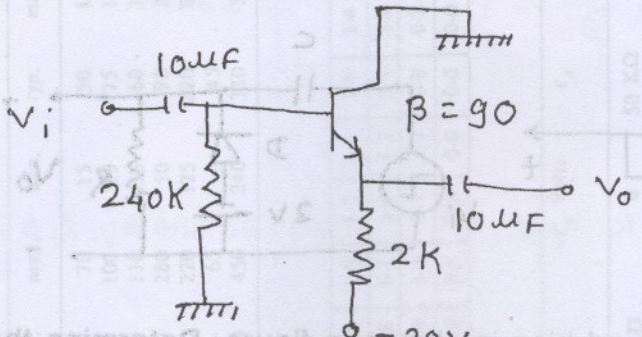
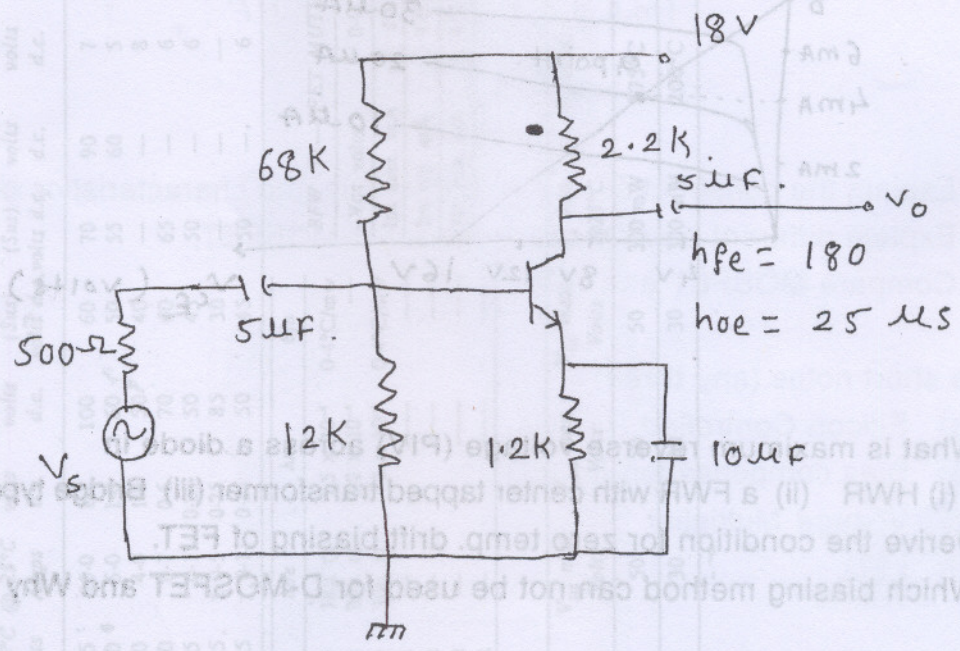
3. (a) Explain the operation of fullwave rectifier and draw the output waveforms for $V_L$dc and $I_L$dc. **10**

(b) Design for a full wave rectifier, an L type LC filter which gives a dc output voltage of 10V at a load current of 100 mA. The allowable ripple factor is 0·02. **10**

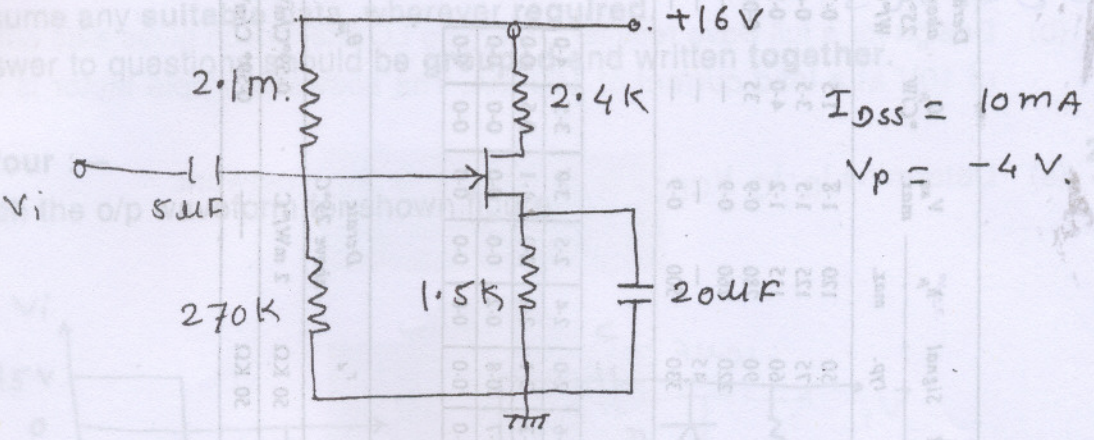
4. (a) Determine I_B, I_C, V_{CEQ}, V_E and V_B for a given network. **10**



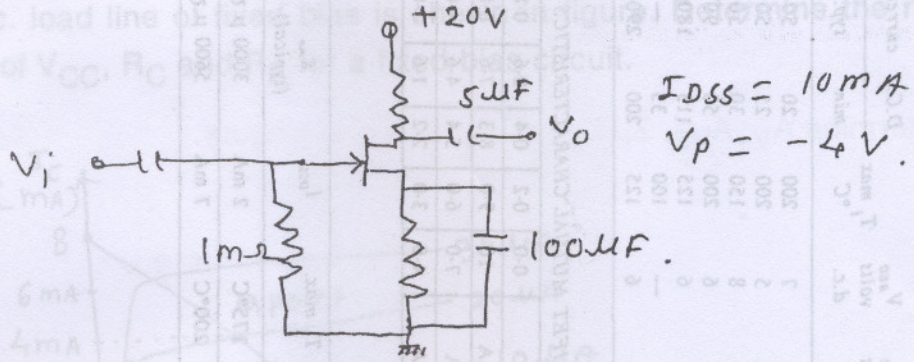
(b) Determine A_V, A_{VS}, Z_i, Z_o and A_I for a given figure. **10**



5. (a) Determine I_{DQ}, V_{GSQ}, V_{DS}, V_S and draw dc load line for the network shown in figure. **10**



(b) Derive the equations for A_V, Z_i and Z_o and determine A_V, Z_i & Z_o for a given network. **10**



6. (a) Explain the construction, working principle and characteristics of D-MOSFET. **10**
   (b) Explain different biasing technique for E-MOSFET. **5**
   (c) Compare MOSFET and FET. **5**

7. Write short notes (any **three**) :— **20**
   (a) Silicon Controlled Rectifier
   (b) Bias compensation for BJT
   (c) Voltage Multiplier
   (d) LED.

DBEC DATA SHEET

Transistor type	Pdmax @ 25°C Watts	Icmax @ 25°C Amps	$V_{CE}^{(sat)}$ volts d.c.	V_{CEO} volts d.c.	V_{CEO} (Sus) volts d.c.	V_{CEX} (Sus) volts d.c.	V_{CEX} volts d.c.	V_{BEO} volts d.c.	T_j max °C	D.C. current gain min	typ.	max.	Small Signal h_{fe} min.	typ.	max.	V_{BE} max.	θ_{fc} °C/W	Derate above 25°C W/°C
2N 3055	115·5	15·0	1·1	100	60	70	90	7	200	20	50	70	15	50	120	1·8	1·5	0·7
ECN 055	50·0	5·0	1·0	60	50	55	60	5	200	25	50	100	25	75	125	1·5	3·5	0·4
ECN 149	30·0	4·0	1·0	50	40	—	—	8	150	30	50	110	33	60	115	1·2	4·0	0·3
ECN 100	5·0	0·7	0·6	70	60	65	—	6	200	50	90	280	50	90	280	0·9	35	0·05
BC147A	0·25	0·1	0·25	50	45	50	—	6	125	115	180	220	125	220	260	0·9	—	—
2N 525(PNP)	0·225	0·5	0·25	85	30	—	—	—	100	35	—	65	—	45	—	—	—	—
BC147B	0·25	0·1	0·25	50	45	50	—	6	125	200	290	450	240	330	500	0·9	—	—

Transistor type	hie	hoe	hre	θja
BC 147A	2·7 KΩ	18μ ℧	$1·5 \times 10^{-4}$	0·4°C/mw
2N 525 (PNP)	1·4 KΩ	25μ ℧	$3·2 \times 10^{-4}$	—
BC 147B	4·5 KΩ	30μ ℧	2×10^{-4}	0·4°C/mw
ECN 100	50Ω	—	—	—
ECN 149	15Ω	—	—	—
ECN 055	12Ω	—	—	—
2N 3055	6Ω	—	—	—

BFW 11—JFET MUTUAL CHARACTERISTICS

−Vgs volts	0·0	0·2	0·4	0·6	0·8	1·0	1·2	1·6	2·0	2·4	2·5	3·0	3·5	4·0
Ids max. mA	10	9·0	8·3	7·6	6·8	6·1	5·4	4·2	3·1	2·2	2·0	1·1	0·5	0·0
Ids typ. mA	7·0	6·0	5·4	4·6	4·0	3·3	2·7	1·7	0·8	0·2	0·0	0·0	0·0	0·0
Ids min. mA	4·0	3·0	2·2	1·6	1·0	0·5	0·0	0·0	0·0	0·0	0·0	0·0	0·0	0·0

N-Channel JFET

Type	V_{DS} max. Volts	V_{DG} max. Volts	V_{GS} max. Volts	P_d max. @25°C	T_j max.	I_{oss}	g_{mo} (typical)	$-V_p$ Volts	r_d	Derate above 25°C	θ_{ja}
2N3822	50	50	50	300 mW	175°C	2 mA	3000 μ ℧	6	50 KΩ	2 mW/°C	0·59°C/mW
BFW 11 (typical)	30	30	30	300 mW	200°C	7 mA	5600 μ ℧	2·5	50 KΩ	—	0·59° C/mW