S 9116

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2006.

Third Semester

Electronics and Communication Engineering

EC 234 — ELECTRONIC CIRCUITS — I

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define an a.c. Load Line.

2. Write short notes on zero current drift in FET.

3. Draw the low frequency equivalent circuit of JFET.

4. Why the Darlington connection is not possible for more number of stages?

5. List any two advantages of transformer coupled class A amplifier circuit.

6. Determine the power handling capacity for 50 W power transistor rated 25°C if derating is required above 25°C at a case temperature of 100°C. The derating factor is 0.25 W/ °C.

7. Write short notes on base-width modulation.

8. A particular optical coupler has a current transfer ratio of 30 percent. If the input current is 100 mA. What is the output current?

9. What P/V rating is required for the diodes in a bridge rectifier produces an average output voltage of 50 V?

10. Define Thermal overload.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Determine V_{CE} and I_C in the voltage-divider biased transistor circuit of fig. 1.

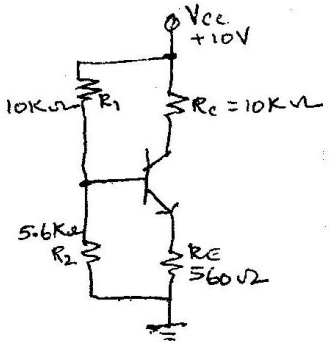


Fig. 1 (12)

(ii) List the advantages of voltage divider biased circuit. (4)

Or

(b) (i) Explain thermistor compensation technique with neat circuit diagram. (8)

(ii) Explain self bias circuit using n-channel JFET. (8)

12. (a) Derive the expression for A_i, A_v, Z_i, Y_o and A_p for transistor amplifier using h parameter model. (16)

Or

(b) (i) Explain Boostrapped Darlington circuit with neat sketch.

(ii) Explain the differential mode operation and common mode operation of transistorised differential amplifier.

13. (a) Explain the push pull class B power amplifier coupled using transformer with neat circuit diagram.

Or

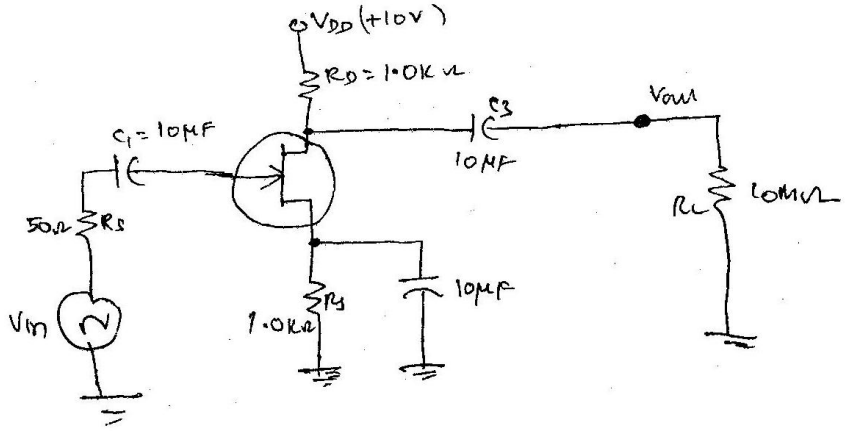
(b) (i) Explain complementary symmetry power amplifier with neat circuit diagram. (10)

(ii) Give the design procedure for heat sinks.

14. (a) Derive the expression for CE short circuit current gain and current gain with resistive load at high frequencies. (16)

Or

(b) Determine the high frequency response of the amplifier circuit shown in fig. 2, C_{iss} =8pF , C_{rss} =3pF and g_m =6500 μS .



15. (a) Describe the working principle of full wave rectifier and derive expression for the ripple factor, rectifier efficiency, V_{DC}, I_{rms}, I_{DC}, V_{rms} and TUF. (16)

Or

(b) Draw the block diagram of SMPs and explain its operation. Discuss its merits and demerits.

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