T.E. (Electronics) (Sem V) (Rev) 29/11/06
Microprocessors & Microcontrollies.

Con. 4994-06. (REVISED COURSE) YM-6688

(3 Hours) [Total Marks : 100

P&D/UPQ/NOV LO E-11-9 37

N. B. : (1) Question Nos. **1** is **compulsory**.
(2) Answer any **four** questions from the remaining questions.
(3) Give proper comments to assembly language programs.
(4) Assume **suitable** data if **necessary**.
(5) Figures to the **right** indicate **full** marks.

1. Design 8086 microprocessor system to meet following requirements. 20
   (a) An 8086 CPU working at 8MHz.
   (b) Co-processor 8087 with the CPU
   (c) 32 KB Monitor Program Area using 2732 chips
   (d) 64 KB Application Program Area using 6264 chips
   (e) 2, 16 Bit input & 2, 16-Bit output, ports, interrupt driven, which are used in variable addressing mode.

   Discuss the design. Draw memory and I/O maps. Use absolute addressing technique in the design.

2. (a) Design a 8051 based microcontroller system with following specifications. 15
   (i) 8051 CPU working at 12 MHz
   (ii) 32 KB Program Memory
   (iii) 32 KB Data Memory
   (iv) 8255 PPI

   Discuss the design.

   (b) Explain following instructions. 5
   (i) MOVX @ DPTR, A (ii) JBC P 1.7, THREE

3. (a) With the help of flow chart explain the interrupt processing sequence of 8086 CPU. 10
   (b) Draw the timing diagram for following machine cycles. 10
   (i) Memory Write (Maximum Mode) m/c.
   (ii) INTA m/c.

4. (a) List and explain the different data types supported by 8087. 8
   (b) What is the purpose of mixed language programming ? Write a mixed language program using ASM - 86 and C to find given year is a leap year or not. 8
   (c) Convert the decimal number – 238.84375 into short real format. 4

5. (a) Write an assembly language program to generate symmetrical square wave on bit ϕ of port 1 using timer zero interrupt of 8051. Assume crystal frequency of 12MHz. 10
   (b) Why PUSH SP instruction is absent in the instruction set of any microprocessor or microcontroller ? 5
   (c) With the help of neat diagram explain internal structure of Port Zero of 8051. 5

6. (a) With the help of detail circuit diagram of single CPU module, explain the operation of loosely coupled configuration. How is the local memory address and global memory address differenciated ? 13
   (b) Draw and explain block diagram of clock generator 8284. 7

7. (a) Why is it not necessary to make odd and even banking while interfacing any kind of ROMS to 8086 ? 5
   (b) What are the internal operations carried out by 8086 CPU upon receiving RESET signal ? 5
   (c) How does NDP (8087) recognise that its master CPU is 8086 or 8088 present in the system ? Why it is necessary for NDP ? 5
   (d) Why RDY input is registered at 2 FF's in 8284 ? 5

8. Write short notes on any **three** :— 20
   (i) IEEE 488 bus standard
   (ii) 8255 PPI.
   (iii) Interrupt structure of 8051
   (iv) Stepper motor interfacing with 8051.