$\overline{R5}$ 

Max Marks: 80

Code No: R5210504

## II B.Tech I Semester (R05) Supplementary Examinations, November 2010 DIGITAL LOGIC DESIGN

(Common to Computer Science & Engineering, Information Technology and Computer Science & Systems Engineering)

Time: 3 hours

Answer any FIVE Questions All Questions carry equal marks

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- 1. (a) Generate Hamming code for the given 11 bit message 10010110101 and rewrite the entire message with Hamming code.
  - (b) The binary numbers listed have a sign bit in the left most position and , if negative numbers are in 2's complement form. Perform the arithmetic operations indicated and verify the answers. [8+8]
    - i. 101011 + 111001
    - ii. 001111 + 110010
    - iii. 111001 011010
    - iv. 101111 100110.
- 2. (a) Write short notes about the various digital logic families.
  - (b) Obtain the complement of the following Boolean expressions.
    - i. AB + A(B + C) + B'(B + D)
    - ii. A + B + A'B'C.
  - (c) Obtain the dual of the following Boolean expressions.

[8+4+4]

- i. A'B + A'BC' + A'BCD + A'BC'D'E
- ii. ABEF + ABE'F' + A'B'EF.
- 3. (a) Construct K-map for the following expression and obtain minimal SOP expression. Implement the function with 2-level NAND -NAND form.  $f(A, B, C, D) = (A + C + D)(A + B + \overline{D})(A + B + \overline{D})(\overline{A} + B + \overline{D})(\overline{A} + B + \overline{D})$ 
  - (b) Implement the following Boolean function F using the two level form:

[8+8]

- i NAND-AND
- ii. AND-NOR  $F(A, B, C, D) = \Sigma 0, 1, 2, 3, 4, 8, 9, 12$
- 4. (a) Implement  $64 \times 1$  multiplexer with four  $16 \times 1$  and one  $4 \times 1$  multiplexer. (Use only block diagram).
  - (b) A combinational logic circuit is defined by the following Boolean functions.

$$F_1 = \overline{ABC} + AC$$

$$F_2 = A\overline{BC} + \overline{A}B$$

$$F_3 = A\overline{B}C + AB$$

Design the circuit with a decoder and external gates.

[8+8]

- 5. (a) Draw the circuit diagram of positive edge triggered D- flip-flop with NAND gates and explain its operation using truth table.
  - (b) Write an HDL behavioural description of a D- flip-flop and D- flip-flop with synchronous preset and clear. [8+8]
- 6. (a) Design a 4-bit ring counter using T- flip flops and draw the circuit diagram and timing diagrams.
  - (b) Draw the block diagram and explain the operation of serial transfer between two shift registers and draw its timing diagram. [8+8]
- 7. (a) Give the HDL code for a memory read , write operations if the memory size is 64 words of 4 bits each. Also explain the code
  - (b) Obtain the 15-bit Hamming code for the 11-bit data word 11001001010.

[8+8]

- 8. (a) i. Explain the difference between asynchronous and synchronous sequential circuits.
  - ii. Define fundamental-mode operation.
  - iii. Explain the difference between stable and unstable states.
  - iv. What is the difference between an internal state and a total state.
  - (b) Explain critical and non critical races with the help of examples.

[8+8]