

Total No. of Questions—12]

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[3862]-164

S.E. (E & TC/Electronics) (I Sem.) EXAMINATION, 2010

DIGITAL LOGIC DESIGN

(2008 COURSE)

Time : Three Hours

Maximum Marks : 100

- N.B. :—** (i) Answer any *three* questions from each Section.
(ii) Answers to the two Sections should be written in separate answer-books.
(iii) Neat diagrams must be drawn wherever necessary.
(iv) Figures to the right indicate full marks.
(v) In Section I : Attempt Q. No. **1 or 2**, Q. No. **3 or 4**, Q. No. **5 or 6**.
(vi) In Section II : Attempt Q. No. **7 or 8**, Q. No. **9 or 10**, Q. No. **11 or 12**.

SECTION I

1. (a) Implement the following function using single 4 : 1 MUX and logic gates : [8]
$$F(A, B, C, D) = \Sigma m(0, 1, 5, 9, 10, 15).$$

(b) Minimize the expression using Quine-Mc-Clusky method : [10]
$$Y = \bar{A}\bar{B}\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D + A\bar{B}\bar{C}\bar{D} + A\bar{B}C\bar{D} + A\bar{B}C\bar{D} + \bar{A}\bar{B}C\bar{D}.$$

Or

2. (a) Design a Gray to BCD code converter using two dual 4 : 1 MUX ICs and some logic gates. [6]
(b) Design even parity generator circuit for 4-bit input using multiplexer. [6]
(c) Design 2-bit comparator using suitable decoder. [6]

P.T.O.

3. (a) Convert : [8]
(1) J-K FF to SR FF
(2) D FF to J-K FF.
- (b) Design a type D counter that goes through states 0, 1, 2, 4, 0, the undesired states must always go to zero (000) on the next clock pulse. [8]

Or

4. (a) Design a pulse train generator using a shift register to generate the following waveform : [8]

(b) Design and implement synchronous modulo 6 Gray code counter using T FF. [8]

5. (a) Compare 'If' and 'Case' statement. Write down the VHDL code for 4 : 1 MUX. (Use behavioural modelling). [8]
- (b) What is the difference between sequential and concurrent statement. [4]
- (c) What is VHDL ? Write entity and architecture declaration for two input NAND gate. [4]

Or

6. (a) Consider a simple example of Half adder. How will you write a VHDL entity declaration for half adder ? Also write an architecture of Half adder in structural style of modelling and data flow style of modelling. [8]
- (b) Write the VHDL code for DFF using synchronous and asynchronous reset input. [8]

SECTION II

7. (a) Design the sequential circuit using J-K FF for the state diagram shown in Fig. 1 : [8]

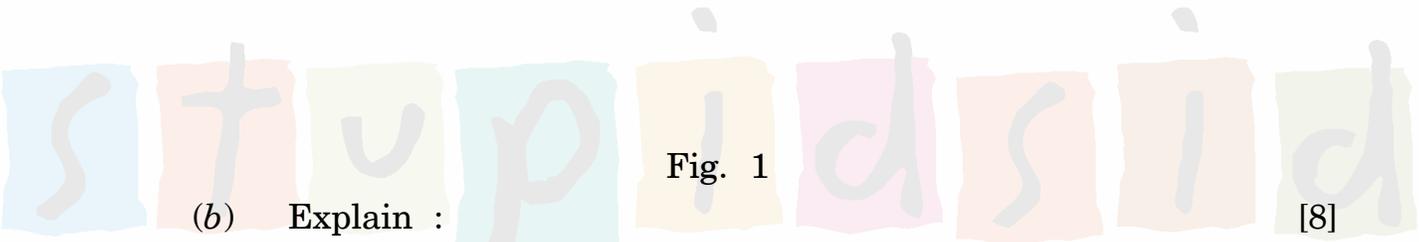


Fig. 1

(b) Explain :

- (1) State table
- (2) State diagram
- (3) Rules for state reduction
- (4) State assignment.

[8]

Or

8. (a) Explain Moore circuit with example. Also compare Moore and Mealy circuit. [8]
- (b) Design a sequence detector to detect a sequence 1101 (Using D FF and Mealy circuit). [8]
9. (a) State merits and demerits of CMOS logic family. Explain with neat diagram two input CMOS and TTL NAND gate. [12]
- (b) Compare TTL, CMOS and ECL. [6]

Or

- 10.** (a) Define the following parameter for digital IC and give their typical values for TTL and CMOS : [10]
- (i) Propagation delay
 - (ii) Noise margin
 - (iii) Fan out
 - (iv) Figure of merit.
- (b) Draw and explain TTL to CMOS and CMOS to TTL interfacing. [8]
- 11.** (a) How to obtained 64×4 memory using 16×4 memory chip ? [8]
- (b) A combinational circuit is defined by the function : [8]

$$F_1(A, B, C) = \Sigma m(4, 5, 7)$$

$$F_2(A, B, C) = \Sigma m(3, 5, 7)$$

Implement this ckt with PLA having 3 input, 3 product terms, and two outputs.

Or

- 12.** (a) What is PLD ? What is the difference btween PAL and PLA ? Explain with the help of a neat diagram. [8]
- (b) What is meant by SRAM and DRAM ? Explain in detail. Also compare SRAM and DRAM. [8]