S.E. (Etrx) Sem 3 (Rev.) Digital Design-I 11/12/07

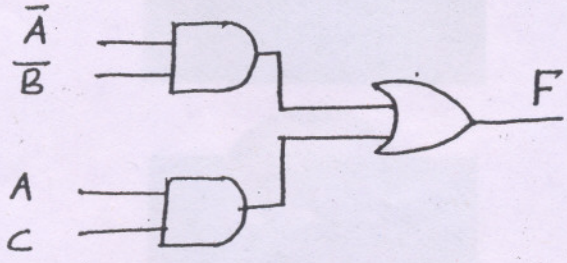
374 : 2ndHf-J

Con. 5485-07. **(REVISED COURSE)** CD-6690

(3 Hours) **[Total Marks : 100**

N.B. (1) Question No. **1** is **compulsory.**
(2) Solve any **four** out of remaining **six** questions.

1. (a) Draw a circuit diagram of 2 i/p TTL NAND gate. Draw its transfer characteristic and explain its operation. 10
(b) Find static hazards in the circuit given below and suggest modification to eliminate the hazard. 10



2. (a) (i) Convert to Hexadecimal number. 10
$(245{\cdot}12)_{10}$
(ii) Solve using 2's Complement method.
$(26)_{10} - (18)_{10}$
(iii) Convert $(341{\cdot}13)_5$ to base 7 number.
(iv) Divide 11011 by 11.
(v) Convert $(A2B3)_H$ to Binary.
(b) Using K map, simplify the following expressions and implement them using NAND gates :— 10
(i) $F(A, B, C, D) = \sum m\ (1, 5, 6, 7, 11, 12, 13) + \sum d\ (10, 15)$
(ii) $F(A, B, C, D) = \sum m\ (0, 2, 5, 7, 8, 10, 13, 15)$.

3. (a) Simplify the following function using Quine McCluskey method :— 10
$F(A, B, C, D, E) = \sum m\ (0, 1, 9, 11, 24, 29, 31) + \sum d\ (8, 15, 30)$.
(b) Implement the function using only one 4 : 1 mux and gates. 10
$F(A, B, C, D) = \sum m\ (0, 2, 3, 6, 8, 9, 11, 13)$.

4. (a) Implement the following functions using active low decoder :— 10
(i) $F(A, B) = \sum m\ (0, 1, 3)$
(ii) $F(A, B) = \pi M\ (0, 2, 3)$ (Do not convert to SOP form).
(b) Explain the features of VHDL and write a program for full adder. 10

5. (a) Implement the following functions using PLA having 3 i/ps, 4 product terms and 2 outputs :— 10
$F_1(A, B, C) = \sum m\ (3, 5, 6, 7)$
$F_2(A, B, C) = \sum m\ (0, 2, 4, 7)$.
(b) Implement BCD adder using 4 bit binary adder IC 7483. Explain its operation by adding 0111 and 0110. 10

6. (a) Draw a logic diagram of JKMS flip-flop. Write its truth table and derive its excitation table. Convert JKMS flip-flop to T flip-flop. 10
(b) Explain the working of comparator IC 7485 and implement 8-bit comparator using the same IC. 10

7. (a) Explain voltage parameters of TTL family. Also explain the current sinking and sourcing when two standard TTL gates are connected. 10
(b) Write short notes on 74180 parity generator and checker IC. 10