S.E. sem 3 (Rev.) Digital system Design-I 12/12/08.

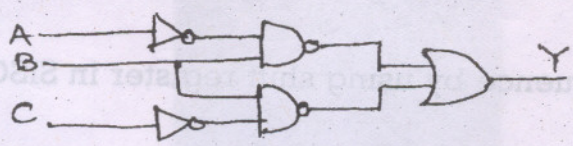
Con. 5736-08. Etrx. **RC-8729**

(REVISED COURSE)

(3 Hours) **[Total Marks : 100**

N.B.: (1) Question no. **1** is **compulsory**.
(2) Solve any **four** from remaining **six** questions.

1. Answer the following questions :— **20**
   (a) Generate a 7 bit even parity hamming code for "1010".
   (b) Simplify the following expression using Boolean theorems
   $(AB+C+D)(\overline{C}+D)(\overline{C}+D+E)$
   (c) Explain lockout condition with the help of 3 bit Ring counter.
   (d) Draw a Karnaugh Map for the given circuit



2. (a) Implement the following function using NAND gates only— **8**
   $F = \Sigma m(1, 2, 4, 7, 11, 13) + d(9, 15)$
   (b) Design a combinational Circuit for controlling panel light of satellite control room. The Light should go ON if :— **12**
   - The pressure in fuel and oxidizer tank is equal to or above the required minimum and there are 10 minutes or less for the satellite to lift off.

   Or

   - The pressure in fuel tank is below the required minimum but there are more than 10 minutes for the satellite to lift off.

   Or

   - The pressure in oxidizer tank is below the required minimum but there are more than 10 minutes for the satellite to lift off.

3. (a) Design a 4:1 MUX with active high enable input using NOR gates only. **10**
   (b) Using Quine McCluskey Simplification Method simplify **10**
   $F = \Sigma m(1, 3, 13, 15) + \Sigma d(8, 9, 10, 11)$

4. (a) Design a 4-bit even parity generator and checker. Implement using one 8:1 MUX each. **10**
   (b) Design a 1 digit BCD adder using IC 7483 and explain the operation for $(0101)_{BCD} + (1001)_{BCD}$ **10**

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5. (a) What are reflective codes ? Give suitable example and explain. 4

(b) Define following parameters for CMOS logic family and give values :— 8

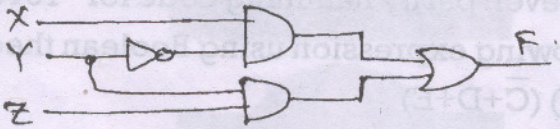
(i) Fan out

(ii) Propagation Delay

(iii) Noise Margin

(iv) Current Parameters.

(c) Find the static hazard in the given circuit and modify it to eliminate the hazard— 8



6. (a) Design a synchronous 4 bit universal up/down counter. 10

(b) Design a MOD 6 asynchronous counter and explain glitch problem. 10

7. (a) Generate "101" sequence by using shift register in SISO mode. Draw timing diagram. 10

(b) Design XY Flip-Flop using JK Flip-Flop :— 10

X	Y	Q_{n+1}
0	0	$\overline{Q}_n$
0	1	Q_n
1	0	1
1	1	0