(3 Hours)   [Total Marks : 100]

N. B. : (1) Question No. **1** is **compulsory**.
        (2) Solve any **four** questions from remaining **six** questions.

1. (a) What are self complementing codes ? Explain with two examples.   20
   (b) Simplify following expression using boolean laws and draw logic diagam using AOI gates.

$$F = A\left(B + C \left[\overline{AB + AC} \right] \right)$$

   (c) If $\overline{Q}$ output of a D–type flipflop is connected to 'D' input, it act as a toggle switch. Verify.
   (d) Implement following expression using 2 : 1 MUX
       $y = \overline{A} + B$, Use 'B' as a select input.

2. (a) Minimize the following logic function using k-Map and realize using NOR gate.   10
       $f (A, B, C, D) = \Sigma m (1, 3, 5, 8, 9, 11, 15) + d (2, 13)$
   (b) A bank Vault has three locks with a different key for each lock. Each key is   10
       owned by different person. In order to open door, at least two people must insert their keys into associated locks. The signal line A, B and C are '1', if there is key inserted into lock 1, 2 and 3 respectively. Write an equation and draw logic diagram for output Z = 1, if door should open.

3. (a) Design 3–bit binary to Gray code converter circuit using 3 line to 8 line decodes   10
       and gates.
   (b) Realize the logic function in SOP form using Quine-mccluskey method.   10
       $f (A, B, C, D) = \pi m (2, 7, 8, 9, 10, 12)$

4. (a) Design 10–bit even parity checker using one 74180 and an Ex-OR gate.   10
   (b) Design a 4–bit Adder/Subtractor circuit using 7483 with ADD/SUB control line.   10

5. (a) Consider M-N Flipflop which is J–K flipflop with an inverter between input K   10
       and external input N.
       (i)   Obtain the characteristics table
       (ii) How to realize D-flipflop from M–N flipflop.
   (b) Define following parameter for CMOS family and gives values.   10
       (i)   Fan out
       (ii) Propagation delay
       (iii) Noise Margin
       (iv) Current parameter.

6. (a) Design mod-10 ripple counter using J–K flipflop and explain slitch problem.   10
   (b) Design mod-5 synchronous counter using J-K flipflop. What happens if the counter   10
       enters in unused state ?

7. (a) Explain working of 4–bit twisted ring counter. Draw its timing diagram.   10
   (b) Explain operation of CMOS NAND gate.   6
   (c) What is static hazards in a combinational digital circuit ?   4