This question paper contains 4 printed pages]

Your Roll No.....

6181

B.Sc. (H) Computer Science/(II Sem.) J

Paper 202–COMPUTER SYSTEM ARCHITECTURE

(N.C. Admission of 2001 and onwards)

Time : 3 *Hours* *Maximum Marks* · 75

(Write your Roll No. on the top immediately on receipt of this question paper)

Attempt *all* questions State the assumptions made in your answers

1. (*a*) How many times does the CPU need to refer to memory when it fetches and executes an indirect address-mode instruction if the instruction is :

(*i*) A computation requiring a single operand

(*ii*) A branch instruction 2

(*b*) What is the function of a Control Unit in a computer? Explain *two* types of control organizations with the help of diagrams. 2+4

(*c*) Give *two* instructions needed in the basic computer in order to set the E flip-flop to 1 ? 2

P.T.O.

(*d*) The memory unit of a computer has 256K words of 32 bits each. The computer has an instruction format with four fields : an operation code field, a mode field to specify one of seven addressing modes, a register address field to specify one of sixty processor registers, and a memory address. Specify the instruction format and the number of bits in each field if the instruction is in one memory word. 5

2. (*a*) Briefly explain the mechanism of next address generation for the control memory with the help of a diagram. 5

(*b*) What is the role of condition and branch fields in a microinstruction ? How many bits are allocated for each ? State the functions designated to all the combinations of these bits. 2+1+4

3. (*a*) Formulate a mapping procedure that provides sixteen consecutive micro-operations for each routine of a basic computer. The opcode was six bits and the control memory has 4096 words. 3

(*b*) Describe the following elements of bus design :

(*i*) Method of arbitration

(*ii*) Bus width 4

(*c*) An addressing field in an instruction placed at memory address 300 contains decimal value 440 The content stored at location 440 is 502 Where is the corresponding operand located for :

(*i*) immediate addressing;

(*ii*) direct addressing

(*iii*) Indirect addressing

(*iv*) register addressing

(*v*) relative addressing 5

4. (*a*) What are the characteristics of RISC and CISC processors ? Is RISC better than a CISC processor ? justify your answer. 4

(*b*) Describe and compare traditional and high performance bus architectures with the help of diagrams. 6

(c) Explain the term 'cycle stealing' with respect to DMA. 2

5. (a) What is Cache Memory ? Name the parameter used to measure the performance of Cache Memory. What is the range of this parameter ? 3

(b) A set associative cache consists of 64 line, or slots, divided into four-line sets. Main memory contains 4K blocks of 128 words each. Show the format of main memory address. 5

(c) For an instruction cycle, draw a six-segment pipeline and its space-time diagram. Assume that the 3rd instruction is a branch instruction. 4

6. (a) Explain Direct Memory Access and give block diagram of DMA controller. How does CPU initialize the DMA transfer ? 6

(b) Compute $(+20)_{10} \times (-13)_{10}$ using Booth's Algorithm. 6