AMIETE – ET (OLD SCHEME)

Code: AE13 **Subject: COMPUTER ENGINEERING**

Time: 3 H DECEMBER 2009 **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2x10)

a. The memory unit for on 80486 micro processor requires _____ banks of memory.

(A) one **(B)** two
(C) three **(D)** four

b. To convert binary to octal & hexadecimal, combine _____ bits

(A) 3 & 4 **(B)** 3 & 3
(C) 4 & 3 **(D)** None of these

c. Architecture of 8086 introduced the concept of _____

(A) pipeline **(B)** flag
(C) segmentation **(D)** all of above

d. Number of output ports in the peripheral mapped I/O is restricted to _____ ports

(A) 16 **(B)** 256
(C) 65536 **(D)** 8

e. Instruction that clears Accumulator is

(A) XRA A **(B)** MVI A, 00
(C) SUB A **(D)** All of above

f. Serial transmission with SIM/RIM instruction work in _____ mode

(A) Asynchronous **(B)** Synchronous
(C) Both **(A)** & **(C)** **(D)** None of above.

g. In 8086 architecture, AX and DS registers belong to
(A) Segment group register, pointer index group register.
(B) Data group register, segment group register.
(C) Segment group register, status flag register.
(D) Data group register, pointer index group register.

h. The VL bus was originally designed to support high speed _____ adapters.

(A) Audio **(B)** Video
(C) Data **(D)** all of above

i. The 8257 DMA controller has _____ channels, and _____ register specify DMA function.
(A) 4, count **(B)** 6, status
(C) 4, status **(D)** 6, count

j. ADD AX, [BX] is an example of _____.

(A) Register indirect-index addressing
(B) Register index addressing
(C) Register addressing
(D) Register indirect addressing.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain how each of the following Microprocessor features affects processing rate :-
(i) Clock frequency
(ii) Data bus width
(iii) Address bus width
(iv) Internal cache memory
(v) Co-processor **(10)**

b. Using 64K x 8 SRAMs, determine the minimum number of chips required to construct a memory interface for 8086 processor. Also design the complete interfacing. **(6)**

Q.3 a. Explain different types of memory and their classification. **(8)**

b. Mention any **TWO** instructions for the following operations:-
(i) Data transfer instruction.
(ii) Logical instruction.
(iii) Arithmetic instruction.
(iv) Input / Output instruction **(8)**

Q.4 a. Draw the architecture of 8086 and label various components. **(6)**

b. Perform the following operations:
(i) Addition with 8-bit two's complement 56+84
(ii) Convert 100001 Binary code to Decimal.
(iii) Address lines = 14, then maximum ____ kB memory can be accessed
(iv) (10000101) bcd = ____ Hexa Decimal code. **(4)**

c. Explain any **TWO** of the following:
(i) Cache memory
(ii) Associative memory
(iii) Virtual memory
(iv) Physical memory **(6)**

(8)

Q.5 Explain the following:
(i) Show the working of the instruction MOV [BP], AL where CS = 5d27, BP = 2c30 and A1 = 05
(ii) How many address lines are used to identity an I/O port in memory mapped I/O methods and peripheral I/O

methods for 8085 architecture?

(iii) CS = 0000H; DS = 2E98H; SS = A010H; ES = B000H. Draw 8086 memory map showing starting and ending of each memory segment.

(iv) Explain the concept of: superscalar, Super – pipeline, L2 cache

(v) Sketch the serial output waveform for character 'A' when it is transmitted with 9600 baud and even parity. **(2+2+3+6+3)**

Q.6 a. Write a note on different modes of 8254 timer. Also show what is the advantage of using 8254 timer for delay routine as compared to software delay routine. **(10)**

b. Write a interrupt service routine to read a data byte and then start conversation for the next reading. **(6)**

Q.7 a. Describe the features of any **TWO** bus architecture:-

(i) ISA
(ii) EISA
(iii) AT
(iv) PCI **(8)**

b. Explain the following operating modes for microprocessors

(i) Virtual mode
(ii) Real mode
(iii) Protected mode **(6)**

c. Explain bus frequency and data transfer rate for VESA bus. **(2)**

Q.8 a. Explain Flynn's classification of computers. **(4)**

b. Explain the following:

(i) Hardware
(ii) Software
(iii) Firmware **(6)**

c. Compare the following:

(i) Distributed and parallel processing.
(ii) Multi-tasking and Multi-processing. **(6)**

Q.9 a. Explain the concept of 'paging' and 'descriptor' in 80386. **(4)**

b. Explain the concept of "pipelining" used in 80486. Show the complete block diagram of it. **(4)**

c. Give an example of any two basic commands used in DOS and UNIX operating system. **(4)**

d. Explain minimum and maximum mode in 8086. **(4)**