ROLL NO. _____

Code: AE27 **Subject: DIGITAL HARDWARE DESIGN**

AMIETE – ET (OLD SCHEME)

Time: 3 Hours **DECEMBER 2011** **Max. Marks: 100**

NOTE: There are 9 Questions in all.

- **Please write your Roll No. at the space provided on each page immediately after receiving the Question Paper.**
- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: **(2×10)**

a. Which of the following converter is used for *quantization*

(A) CAD **(B)** DAC
(C) CDA **(D)** ADC

b. In *Gray code*, bit-vectors corresponding to consecutive digit values differ by

(A) 4-bits **(B)** 5-bits
(C) 1-bit **(D)** 2-bit

c. Each time an event occurs on any of the signals in the sensitivity list, the statements within a ---------- are executed in a sequential order.

(A) procedure **(B)** process
(C) function **(D)** block

d. Logic blocks, interconnection switches and I/O blocks are features of

(A) PLA **(B)** ROM
(C) PSA **(D)** FPGA

e. The number of decoder modules in a coincident decoder are

(A) 2 **(B)** 4
(C) 8 **(D)** 16

f. The output function of Moore machine is given by:

(A) $z(t) = H(S(-t))$ **(B)** $z(t) = H(S(t))$
(C) $z(t) = H(S(-t), x(t))$ **(D)** $z(t) = H(S(t), x(t))$

g. ------ module is the *control unit* of microprogrammed controller.

(A) Control-store address register **(B)** Control-store address generator
(C) Microcontroller **(D)** Control store

h. A switching function is said to be ---------- if and only if it is invariant under any permutation of its variables.

(A) symmetric **(B)** unate
(C) cannonical **(D)** threshold

i. If the width of the trigger pulse is greater than the propagation time of the flip-flop, then flip-flop continues to toggle and results in unpredictable output. This feature is known as

(A) race around condition **(B)** unknown condition
(C) stuck around condition **(D)** None of the above

j. Datapaths provide connection between various components in a data sub-system consisting of --------

(A) switches and storage modules **(B)** wires and functional modules
(C) switches and functional modules **(D)** wires and switches

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain module level, logical level and physical level of implementation in a digital system. **(5)**

b. Mention any five features of high level specification of combinational systems. **(5)**

c. Explain the following features in combinational systems:
(i) Karnaugh's map
(ii) Tabulation method **(3+3 = 6)**

Q.3 a. Describe a system that counts the number of 1's in a four-bit vector *x*. Give the following:
(i) High-level using arithmetic expression
(ii) Table of arithmetic expression **(5)**

b. Reduce the following switching expression to 4 literals:
$abc\square d + ab\square c + bc\square d + ab\square c\square + acd + a\square bcd$ **(3)**

c. Mention any two features of the following:
(i) Methods to minimize a switching functions
(ii) Symmetric function
(iii) Threshold logic
(iv) Unate function **(8)**

Q.4 a. Expand the features of VHDL. Explain how entity and architectures are related with a block diagram. **(3+4)**

b. Give an example to illustrate mixed style modeling using VHDL. **(6)**

c. Compare functions and procedures in VHDL. **(3)**

Q.5 a. Explain coincident decoding and tree decoding used in decoder networks. **(8)**

b. What is a shift register? Explain various types of shift registers and give their respective applications. **(8)**

Q.6 a. Compare Moore and Mealy state machines. Give their applications. **(6)**

b. Explain any two methods used in simplification of incompletely specified synchronous machines. **(6)**

c. Explain the asynchronous state machine and its mode of operations. **(4)**

Q.7 a. Explain data subsystem. Mention various components used in data subsystem. Explain the role of storage and functional modules in data subsystem. **(8)**

b. Write short notes on ASM Charts. **(4)**

c. Compare explicit and implicit microinstruction sequencing. **(4)**

Q.8 a. Determine the state diagram for the sequential system described by the following expressions: **(6)**

$$s(t+1)=\begin{cases} s(t) & \text{if } x=a \\ (s(t)+1) \bmod 5 & \text{if } x=b \\ 2 & \text{if } x=c \end{cases}$$

$$z(t)=\begin{cases} 0 & \text{if } s(t) \text{ is even} \\ 1 & \text{otherwise} \end{cases}$$

The system has five states labeled 0,1,2,3, and 4.

b. Give the advantages and disadvantages of programmable modules. **(6)**

c. Explain various types of hazards in asynchronous sequential circuits. **(4)**

Q.9 a. Write short notes for any **THREE** of the following:

(i) Microinstruction format
(ii) Microinstruction timing
(iii) Signal and variables in VHDL
(iv) Priority Encoders **(3×4 = 12)**

b. Express the complement of $E(x, y, z) = \Pi M(1,4,6,7)$ as sum of minterms and product of maxterms. **(4)**