C13-R3: DIGITAL SYSTEM DESIGN

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) Derive the truth table for the following equation:

$$F(A,B,C) = (A+B)' \oplus (B' C)' + (AB)$$

b) You need a JK flip-flop for your new digital system design, but all you have available is a D-type flip-flop and a small amount of logic gates. Design the logic necessary to convert the D-type flip-flop to a JK flip-flop.

c) Assume that the exclusive-OR gate has a propagation delay of 10 nanoseconds and the AND and OR gates have a propagation delay of 5 nanoseconds. What is the total propagation delay time in the 4-bit Ripple Carry Adder?

d) What is the major difference between a combinational circuit and a sequential circuit? What additional circuit components are employed in a sequential circuit?

e) Suppose that a CMOS microprocessor operating at 4 Volts and running at 100MHz consumes 10 Watts. For the next release, the manufacturer considers decreasing the voltage to 2 Volts while increasing the frequency to 1GHz. Everything else about the microprocessor stays the same. Estimate the power that will be consumed by the new processor.

f) Describe the difference between a PAL and PLA. Name one possible disadvantage of using PLA or PAL to implement logic vs. implementing logic with dedicated gates.

g) Assuming that the shift register shifts to the right give a state diagram for a 3-bit shift register.

(7x4)

2.

a) The following truth table describes a three-input combinational logic function:

a	*b*	*c*	*z*
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

Write down a Boolean expression for the output of this function in sum of products (OR of AND terms) form. Can your expression be reduced to a simpler sum of products form? What are the advantages and disadvantages of sum of products circuits for implementing combinational logic functions?

b) Design a combinational circuit that reverses a 4-bit number. In a bit reverse instruction, the most significant bit becomes the least significant bit. The next most significant bit becomes the next least significant bit, and so on until the least significant bit becomes the most significant bit in the result. For example, 1101 becomes 1011.

(9+9)

3. Minimize the following functions using K-maps. Give your answer in POS form.

a) $f = \Sigma\,(1, 4, 5, 9, 11, 14) + d(0, 2, 7, 8, 13)$

b) $f = \Sigma\,(2, 7, 10, 11, 14) + d(1, 4, 6)$

(9+9)

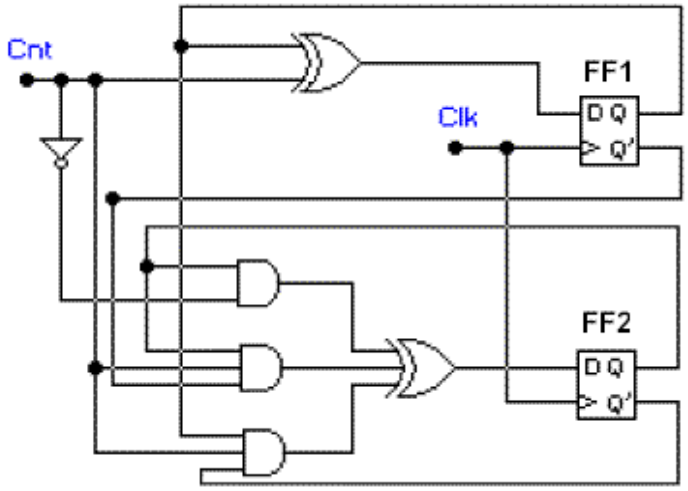
4.

a) Design an asynchronous counter with the following count sequence 9-8-7-6-5-4-3-2-9-8, etc. Use positive edged triggered TFF.

b) Design a full adder using the attached PLA and PAL.

(9+9)

5. Derive the state table and state diagram for the sequential circuit shown in Figure below.



(18)

6. Implement the following function with a 8x1 multiplexer. Use variable **A** as one of the inputs.

F (A, B, C, D)= Σ(2, 5, 6, 7, 10, 11, 12, 13)

(18)

7. A datapath has five major components, C_1 through C_5, attached in a loop. The maximum delay of each of these components is as follows: C_1 = 2 ns; C_2 = 1 ns; C_3 = 3 ns; C_4 = 4 ns; and C_5 = 4 ns.

a) What is the maximum clock frequency that can be used for this datapath?

b) The datapath is to be modified to one that is pipelined using three stages. How should the components be combined into stages and what is the maximum clock frequency that can be achieved?

c) Repeat b) above for four pipeline stages.

(8+6+4)