Total No. of Questions—12] [Total No. of Printed Pages—4+2

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S.E. (E&TC/Electronics) (I Sem.) EXAMINATION, 2010

DIGITAL LOGIC DESIGN

(2008 COURSE)

Time : Three Hours **Maximum Marks : 100**

N.B. :— (*i*) Answers to the two Sections should be written in separate answer-books.

(*ii*) Neat diagrams must be drawn wherever necessary.

(*iii*) Figures to the right indicate full marks.

(*iv*) Assume suitable data, if necessary.

(*v*) In Section I : Attempt Q. No. **1** *or* Q. No. **2**, Q. No. **3** *or* Q. No. **4**, Q. No. **5** *or* Q. No. **6**.

In Section II : Attempt Q. No. **7** *or* Q. No. **8**, Q. No. **9** *or* Q. No. **10**, Q. No. **11** *or* Q. No. **12**.

SECTION I

1. (*a*) Simplify the following Boolean function by using a Quine-McClusky method

$F(A, B, C, D) = \Sigma m(0, 2, 3, 6, 7, 8, 10, 12, 13)$. [10]

P.T.O.

(b) Why is Gray code used for labelling the cells of K-map. [4]

(c) Write a short note on ALU. [4]

Or

2. (a) Design a logic circuit which has three inputs A, B, C and gives a high output when majority of inputs is high. [6]

(b) Draw logic circuit of a 4 : 1 multiplexer and explain its working. [6]

(c) Design a full adder using 3 : 8 decoder and NAND gates. [6]

3. (a) Explain the difference between combinational and sequential circuits.

Also convert JK Flip-Flop into D flip-flop and T flip-flop. [8]

(b) Design and implement a mod-10 asynchronous counter using T Flip-Flops. [8]

Or

4. (a) Explain the operation of a master-slave JK Flip-Flop and show how the race around condition is eliminated in it. [6]

(b) Design mod-6 synchronous counter using JK Flip-Flops and implement it. [6]

(c) Explain how shift registers are used as :

(i) Serial to parallel converter

(ii) Parallel to serial converter. [4]

5. (a) Describe different modelling styles of VHDL with suitable examples. [8]

(b) Write a VHDL code to design a BCD to seven segment decoder for a single digit LED display. [8]

Or

6. (a) Explain different classes of data objects in VHDL with example for each. [8]

(b) Explain the following statements used in VHDL with suitable example :

(i) Process

(ii) If

(iii) With select

(iv) Wait. [8]

SECTION II

7. (*a*) Draw and explain block diagram of Mealy and Moore machine. [6]

(*b*) Write short notes on :

(*i*) State diagram

(*ii*) State table

(*iii*) State reduction

(*iv*) State assignment. [8]

(*c*) What does the word 'Finite' signify in the terms finite state machine ?

State advantages and disadvantages of a finite state machine. [4]

Or

8. (*a*) Design a sequential circuit using Mealy machine for detecting overlapping sequence 1101. Use JK Flip-flops. [8]

(*b*) Explain ASM chart notations in detail. [6]

(*c*) What is the difference between conventional flow charts and ASM charts ? [4]

9. (*a*) With the help of neat circuit diagram explain the working of :

(*i*) A two-input TTL NAND gate

(*ii*) A two-input CMOS NOR gate. [10]

(*b*) What is meant by open collector output of TTL gate ? What is its utility ? Draw the circuit showing open collector output and pull up resistor. [6]

Or

10. (*a*) Explain the following characteristics of TTL logic families :

(*i*) Power dissipation

(*ii*) Noise margin

(*iii*) Propagation delay

(*iv*) Fan out. [8]

(*b*) Describe what happens to each of the following CMOS characteristics as V_{DD} is increased :

(*i*) Noise margin

(*ii*) Power dissipation

(*iii*) Switching speed.

And in which applications is CMOS ideally suited ? [8]

11. (*a*) State various characteristics of memory devices and explain in brief any *two*. [6]

(*b*) A combinational circuit is defined by the function :

$F_1(A, B, C) = \Sigma m(1, 5, 7)$

$F_2(A, B, C) = \Sigma m(5, 6, 7)$

Implement the circuit with a PLA. [6]

(*c*) Give the comparison between PROM, PLA and PAL. [4]

Or

12. (*a*) Differentiate between static and dynamic RAM. Draw circuits of one cell of each and explain its working. [8]

(*b*) Obtain a 2048 × 8 memory using 256 × 8 memory chips. [6]

(*c*) Distinguish between volatile and non-volatile memories. [2]