

Total No. of Questions—12]

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**[3862]-213**

**SE. (Comp. Engg.) (First Semester) EXAMINATION, 2010**

**(Common to Computer and I.T.)**

**DIGITAL ELECTRONICS AND LOGIC DESIGN**

**(2008 COURSE)**

**Time : Three Hours**

**Maximum Marks : 100**

**N.B. :—** (i) Answer Q. No. 1 or 2, Q. No. 3 or 4, Q. No. 5 or 6 from Section I and Q. No. 7 or 8, Q. No. 9 or 10, Q. No. 11 or 12 from Section II.

(ii) Answers to the two sections should be written in separate answer-books.

(iii) Neat diagrams must be drawn wherever necessary.

(iv) Figures to the right indicate full marks.

### **SECTION I**

1. (a) Design and explain in detail 4-bit input grey code to 7-segment BCD code conversion technique. For this design use K-map reduction and MSI circuit for each segment of display. [16]
- (b) Enlist various code conversion methods. [2]

*Or*

2. (a) Express the following numbers in binary format. Write step by step solution. [12]
- (i)  $(7762)_{\text{octal}}$

P.T.O.

(ii)  $(432A)_{\text{hex}}$

(iii)  $(2946)_{\text{decimal}}$

(iv)  $(1101.11)_{\text{decimal}}$ .

- (b) What will max. 4-digit equivalent Hex number for 4-digit max. Decimal number ? Also perform the following subtraction : [6]

$$(7048)_{\text{Decimal}} - (07A8)_{\text{Hex.}}$$

3. (a) Solve the following using K-map reduction technique. Also draw MSI circuit for output. [12]

(i)  $Z = f(A, B, C, D) = \pi (1, 2, 3, 9, 10, 12, 15)$

(ii)  $Z = f(A, B, C, D) = \pi (0, 2, 3, 4, 6, 8, 11, 13).$

- (b) Explain for IC 74LSXX various characteristics in brief. [4]

Or

4. (a) Draw and explain the design of 3-I/P TTL NAND gate circuit. Also explain various I/P, O/P states and corresponding transistor (ON/OFF) states. [12]
- (b) Explain working of 2-input CMOS-NOR gate. [4]

5. (a) Explain the working of cascaded mode magnitude comparator IC 7485. [8]
- (b) Draw and explain 4-bit BCD adder using IC 7483. Also explain with reference to your design addition of  $(9 + 5)_{\text{BCD}}$  and  $(7 + 2)_{\text{BCD}}$ . [8]

*Or*

6. (a) Explain decoder (1 : 8) as full adder and full subtractor. Show your design. [8]
- (b) Design 28 : 1 mux using 8 : 1 mux (with enable inputs). Explain truth table of your design in short. [Hint : you can use separate mux for enable of respective IC's] [8]

## SECTION II

7. (a) Draw a 4-bit synchronous counter. Also explain timing diagram for the same. [10]
- (b) What is the advantage of M-S flip-flop ? Explain working of MS J-K flip-flop in detail. [8]

*Or*

8. (a) What is advantage of MOD counter ? Explain working of MOD-17 and MOD-24 counter with detail diagram using IC-7490. [8]
- (b) Explain ring counter with design having initial state '01011', from initial state explain all possible states in that ring. [10]
9. (a) What is VHDL ? Explain entity-architecture declaration for 2-bit NOR and AND gate. [8]
- (b) What is ASM chart ? Design ASM chart for 4-bit grey code sequence with up-down conditions. [8]

*Or*

- 10.** A sequential ring counter with present state '01011'. The circuit also have an input 'Z'. If  $Z = 0$ , circuit shows next-output (right shift) else for  $Z = 1$ , it shows initial state. Draw an ASM chart and state stable for this circuit to generate the output using mux controller method. [16]
- 11.** (a) Explain difference between FPGA and CPLD logic. [8]  
(b) Explain machine cycle of an addition operation of a micro-processor. Use two 8-bit numbers to explain the same. [8]

*Or*

- 12.** (a) Explain in brief the function of Address bus, Data bus and control bus for a basic microprocessor. [8]  
(b) Explain in brief design model of PLA for any code conversion example. [8]