S.E. (E&TC) (Sem. III) (Rev.) Dec. 07

Electronic Circuits analysis and Design

15/12/07

Co². 5127-07.

(REVISED COURSE)

CD-6699

(3 Hours)

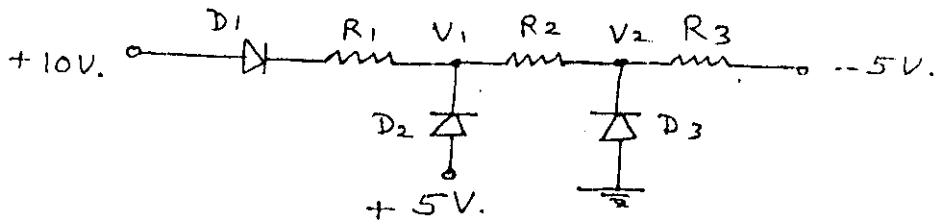
[Total Marks : 100

N.B. (1) Question No. 1 is **compulsory.**
(2) Attempt any **four** questions from remaining.
(3) **Figures** to the **right** indicate **full** marks.
(4) Assume additional **data** wherever **necessary.**

1. Solve any **four** of the following :— 20

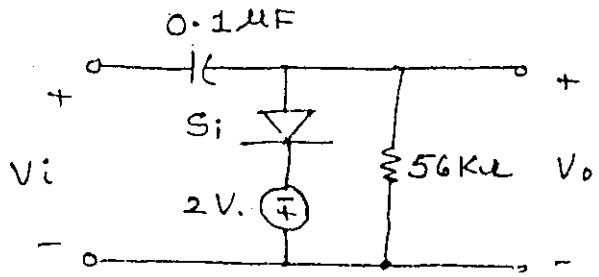
(a) n-channel, CS, JFET amplifier with self-biased circuit configuration with R_S bypassed is desired to bias for zero drain current drift. If R_D = 10 KΩ, V_P = –2·0 V, g_{mo} = 1·6 mA/V and I_{DSS} = 1·65 mA. Find —
(i) I_D for zero drift, (ii) V_{GS}, (iii) R_S, (iv) A_V.
Assume V_{DD} = 24 V.

(b) The cut-in voltage for each diode is 0·6 V. Determine V_1 and V_2 and each diode current if R_1 = 2 KΩ, R_2 = 6Ω, R_3 = 2 KΩ.



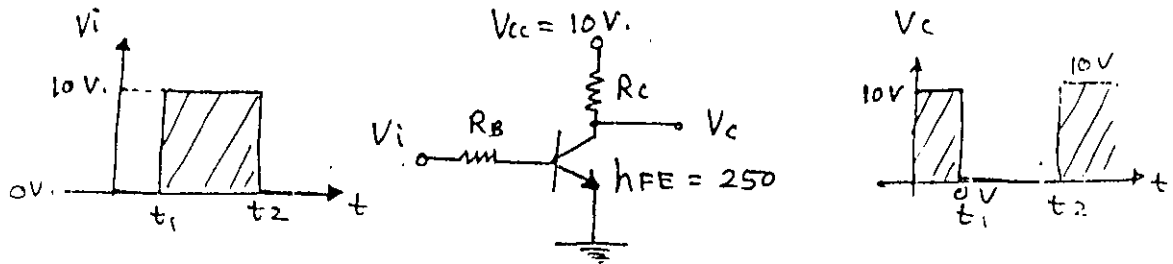
(c) Compare common base, common collector and common emitter BJT amplifiers.

(d)



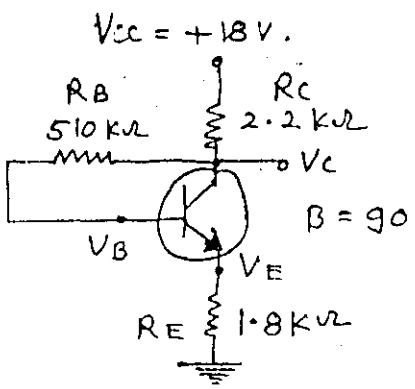
For the given network find 57 of the circuit, compare it with half the period of applied signal and sketch V_o if V_i is 20 V P–P, square wave, 1 kHz waveform.

(e) Determine R_B and R_C for the transister inverter if I_C sat = 10 mA.



(f) Compare 'L' and 'C' filter.

2. a) Answer the following questions about the circuit shown :— 10



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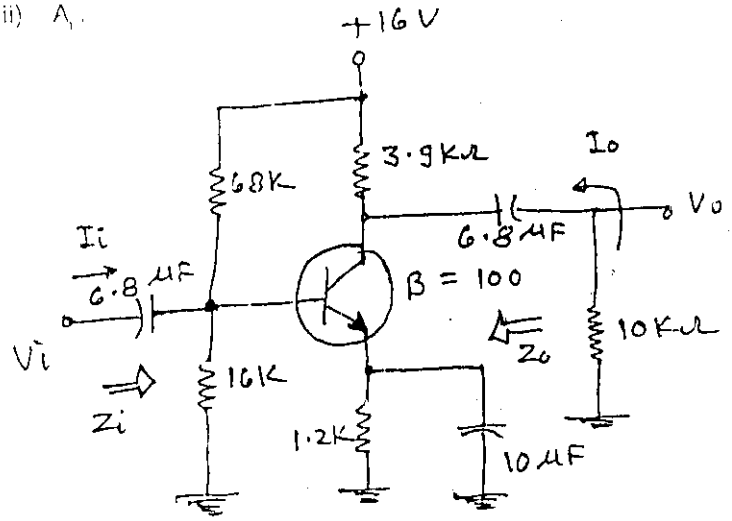
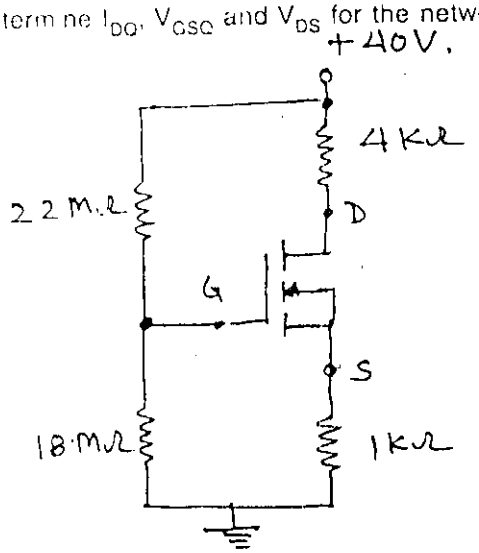
(i) What happens to the voltage V_C if resistor R_B is open.
(ii) What should happen to V_{CE} if B increases due to temperature.
(iii) How will V_E be affected when R_E is replaced with one whose resistance is at the lower end of the tolerance range ?
(iv) If transistor collector connection becomes open, what will happen to V_E ?
(v) What might cause V_{CE} to become nearly 18 V. 10

(b) For the given circuit find :—
(i) Determine Z_i, Z_o and A_v no load
(ii) A_v with load
(iii) A_i.



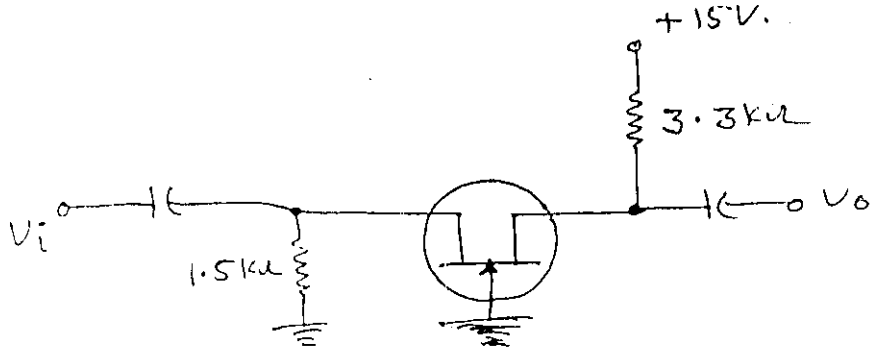
3. (a) Determine I_{DQ}, V_{GSQ} and V_{DS} for the network shown :— 10



2N4351
V_{GS} (TH) = 5 V
I_D(on) = 3 mA
at V_{GS} (on) = 10 V.

Use graphical method.

(b) Determine Z_i, Z_o and V_o if V_i = 0·1 mV repeat the same if γ_d = 25 KΩ. 10



I_{DSS} = 8 mA
V_p = −2·8 V
γ_d = 40 KΩ

Design a single stage CS JFET amplifier using Potential Divider Biasing for the following specifications :— 20

V_o = 2 V, f_L = 20 Hz

I_D = 3·3 ± 0·6 mA

$|A_v|$ = 11

Use BFW11.

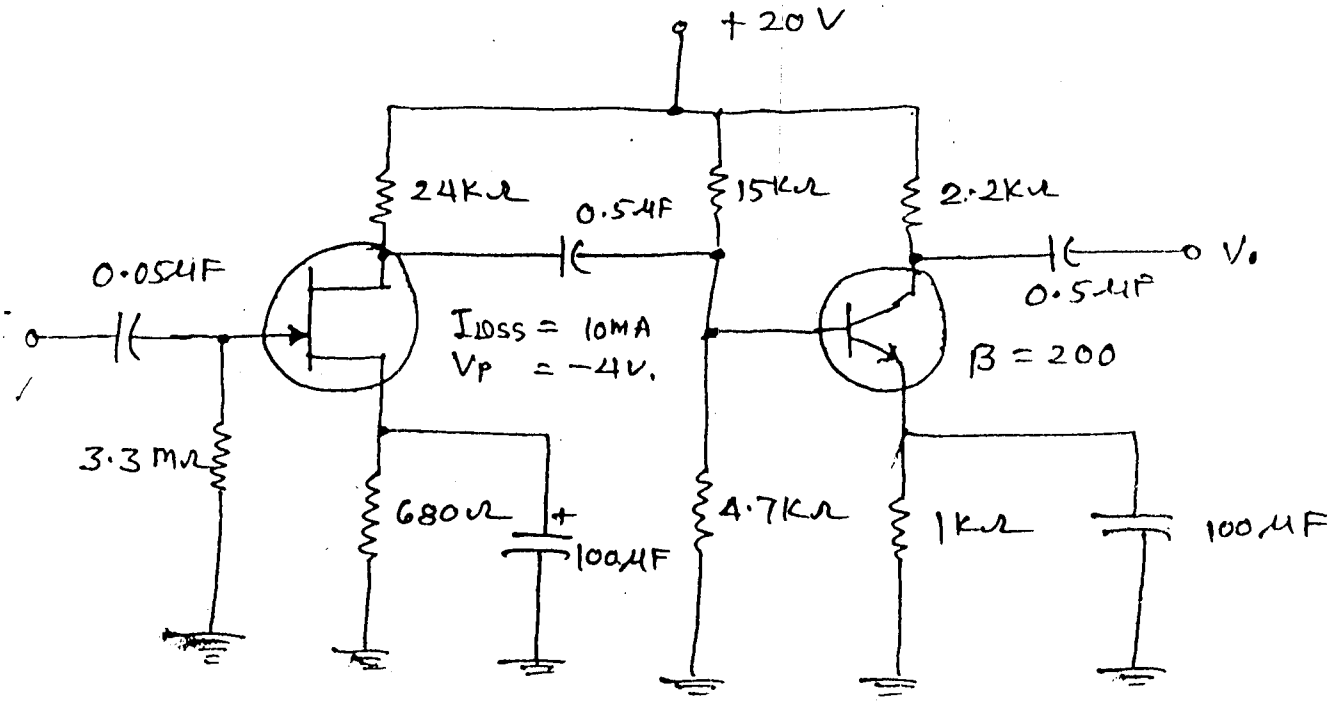
Calculate R_i, R_o and $V_{o\ (max.)}$ for the designed amplifier.

Design a single stage CE BJT amplifier using BC147A to satisfy the following specifications :— 20

$|A_v| \geq 120$, $SI_{co} \leq 8$, V_{cc} = 24 V, R_L = 10 KΩ, f_L > 10 Hz, I_{CQ} = 3 mA.

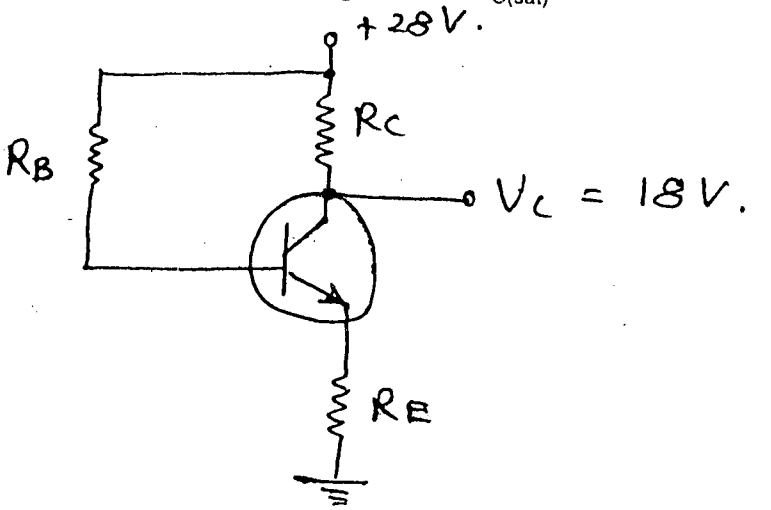
Estimate R_i and R_o of designed amplifier. If $R_i \geq 3$ KΩ is new specification then suggest suitable modifications in above design. What sacrifices you have made ? Calculate that.

a) For the Cascade amplifier shown calculate input impedance, output impedance, voltage gain and resulting output voltage if V_i = 1 mV sine wave of 2 KHz. 14



Determine R_C, R_E and R_B if the specifications for the given circuit is — 6

$I_{CQ} = \frac{1}{2} I_{C\ (sat.)}$, V_{CC} = 28 V, V_C = 18 V, $I_{C(sat)}$ = 8 mA, B = 110.



Write short notes on any **four** of the following :— 20

a) Various biasing schemes for E-MOSFET

b) Solar Cells : Working, characteristics and applications

c) Transistor as a constant current source

d) Diode clipping circuits : Working and waveforms

e) Hybrid π equivalent circuit of a BJT

f) Schottky Diode : Construction, working and special features, V-I characteristics.
