JUNE 2009

AMIETE – ET (OLD SCHEME)

Code: AE09
Subject: ANALOG & DIGITAL ELECTRONICS
Time: 3 Hours
Max. Marks: 100

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2 ×10)

a. CMRR is defined as

(A) $20\log\frac{|A_d|}{|A_c|}$. **(B)** $20\log\frac{|A_c|}{|A_d|}$.

(C) $10\log\frac{|A_d|}{|A_c|}$. **(D)** $10\log\frac{|A_c|}{|A_d|}$.

b. An Op-amp has

(A) High input impedance and high output impedance.
(B) High input impedance and low output impedance.
(C) Low input impedance and high output impedance.
(D) Low input impedance and low output impedance.

c. The magnitude function of an N^{th} order Butterworth filter with a passband edge ω_p is given by

(A) $|H(j\omega)| = \frac{1}{\sqrt{1+\varepsilon^2\left(\frac{\omega}{\omega_p}\right)^N}}$. **(B)** $|H(j\omega)| = \frac{1}{\sqrt{1+\varepsilon^2\left(\frac{\omega_p}{\omega}\right)^N}}$.

(C) $|H(j\omega)| = \dfrac{1}{\sqrt{1+\varepsilon^2\left(\dfrac{\omega_p}{\omega}\right)^{2N}}}$. **(D)** $|H(j\omega)| = \dfrac{1}{\sqrt{1+\varepsilon^2\left(\dfrac{\omega}{\omega_p}\right)^{2N}}}$.

d. The Q-factor for parallel LCR resonator is

(A) $Q = \omega_0 CR$. **(B)** $Q = \dfrac{\omega_o}{CR}$.

(C) $Q = \omega_0 LC$. **(D)** $Q = \dfrac{\omega_o}{LC}$.

e. In Schottky barrier diode, junction is formed by

(A) metal-extrinsic semiconductor.
(B) metal-intrinsic semiconductor.
(C) Two dissimilar metals.
(D) Extrinsic and intrinsic semiconductor.

f. A CMOS logic gate consist of

(A) NMOS and PMOS transistors.
(B) Two NMOS or two PMOS transistors.
(C) n-p-n and p-n-p transistors.
(D) Two n-p-n or p-n-p transistors.

g. _____ used for impedance matching.

(A) Inverting amplifier
(B) Non-inverting amplifier
(C) Voltage follower
(D) Logarithmic amplifier

h. Major limitation of FET over BJT is

(A) Higher input impedance.
(B) Lower gain-bandwidth product.
(C) Higher effect of diffusion capacitance.
(D) Higher effect of depletion capacitance.

i. NMOS is preferred over PMOS because

(A) Electron diffuses faster than holes.
(B) Mobility of electron is higher than hole.
(C) Easy to fabricate.

(D) Lower cost.

j. Universal gates are

(A) AND, OR and NOT gates.
(B) XOR and XNOR gates.
(C) RTL and TTL gates.
(D) NAND and NOR gates.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Draw and explain CMOS Op-amp. **(8)**

b. Design the instrumentation amplifier and obtain its output voltage. **(8)**

Q.3 a. Design a 4-bit bi-directional shift register and explain it. **(8)**

b. Design a 4 bit up-down ripple counter and explain it with appropriate logical waveform. **(8)**

Q.4 a. Find the order and transfer function of the Butterworth LPF whose specification as follows: f_p =10 KHz, f_s = 50 KHz, A_{max} =1 dB, A_{min} =20 dB and DC gain is unity. **(10)**

b. Derive an expression for the transfer function of the 2nd order notch filter. **(6)**

Q.5 a. What is switched-capacitor filter? Explain the operation with a practical circuit. **(8)**

b. Explain the dual-slope ADC with suitable diagram. **(8)**

Q.6 a. Implement the Full Adder using 8 x 1 Multiplexers. **(8)**

b. Draw and explain the logarithmic amplifier with suitable mathematical relation. **(4)**

c. Draw and explain logarithmic multiplier of two analog signals. **(4)**

Q.7 a. Explain diffusion capacitance and transition capacitance. **(4)**

b. How do you ensure that faster switching operation being made using Schottky diode in transistor circuit? **(2)**

c. Explain the switching characteristics of diode using suitable diagram. **(10)**

Q.8 a. Explain: Noise margin, Propagation delay, Power dissipation, Delay-power product, Fan-in and Fan-out. **(10)**

b. Explain the operation of the NMOS transistor as a switch in the implementation of pass-transistor logic circuit. **(6)**

Q.9 a. Explain the operation of basic TTL NAND gate. **(8)**

b. Compare static RAM with dynamic RAM. **(8)**