

This question paper contains 4 printed pages ]

Your Roll No

**6178**

**B.Sc.(Hons.) Computer Science / I Sem. J**

**Paper 104 : DIGITAL ELECTRONICS**

**(Admissions of 2001 and onwards)**

**Time : 3 Hours**

**Maximum Marks : 75**

*(Write your Roll No on the top immediately on receipt of this question paper.)*

**Attempt all questions**

**Parts of a question must be answered together**

- 1 (a) What is the radix (base) that satisfies the following equation ?  
 $(53)_r + (120)_r = (213)_r$  2
- (b) Generate decimal codes for 5 3 2 -1 code as a self complementing weighted code 3
- (c) Convert  $(25)_{10}$  and  $(60)_{10}$  into equivalent binary Then perform  $(25)_{10} - (60)_{10}$  using 2's complement method 3
- (d) Show that a positive logic NAND gate is a negative logic NOR gate and vice-versa 2

- (e) Given the 8-bit data 10010110, generate a 13-bit composite word for the hamming code that corrects single error and detects double error 2
- (f) In a  $2K \times 8$  memory, determine 3
- (i) number of address lines
  - (ii) number of data lines
  - (iii) specify its bit capacity
- 2 (a) Simplify the following Boolean function using tabulation method 8
- $f = \Sigma (0, 8, 24, 32, 33, 41, 48, 56)$
- $d = \Sigma (16, 17, 40, 57)$
- (b) Draw the logic diagram of a  $2 \rightarrow 4$  line decoder using only NOR gates. Include an enable input 4
- 3 (a) Simplify the given function using NAND-NAND logic 4
- $f(A, B, C, D) = \pi (1, 3, 5, 7, 13, 15)$
- (b) Implement a full subtractor with two  $4 \times 1$  multiplexers 4
- (c) Construct a  $16 \times 1$  multiplexer with two  $8 \times 1$  multiplexer and one  $2 \times 1$  multiplexer. Use only block diagrams 4

- (b) Describe the internal architecture of ROM that store 4K bytes and uses a square register array 4
  - (c) Explain static hazards in combinational circuit (with example) 2
  - 6 (a) Draw the circuit of 4-bit binary ripple down counter using J-K flip-flops 4
  - (b) Design a combinational circuit that converts excess-3 decimal code to 2421 decimal code 8
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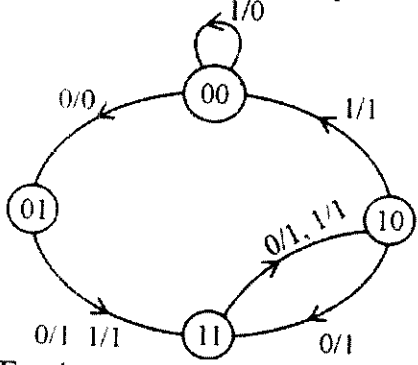
- 4 (a) A new flip-flop namely DUMB has 2 inputs (x & y) with the characteristic table as

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| x | y | $\theta(t+1)$     |
|---|---|-------------------|
| 0 | 0 | $\bar{\theta}(t)$ |
| 0 | 1 | 1(set)            |
| 1 | 0 | reset             |
| 1 | 1 | $\theta(t)$       |

Find its characteristic equation and excitation table

- (b) Design it using D-flip-flop and logic gates



For this state diagram, design a circuit using J-K flip-flops and logic gates

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- 5 (a) Determine the minimal state table that is equivalent to the following state table

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| P S | N S , output |       |
|-----|--------------|-------|
|     | Input x = 0  | x = 1 |
| A   | F, 0         | C, 0  |
| B   | H, 1         | A, 1  |
| C   | H, 0         | D, 1  |
| D   | B, 0         | H, 0  |
| E   | G, 0         | C, 0  |
| F   | C, 1         | E, 1  |
| G   | H, 1         | E, 1  |
| H   | C, 0         | A, 1  |