CE1-R3: ADVANCED COMPUTER ARCHITECTURE

NOTE:

1. **Answer question 1 and any FOUR questions from 2 to 7.**
2. **Parts of the same question should be answered together and in the same sequence.**

Time: 3 Hours **Total Marks: 100**

1.

a) What are the limitations of Instruction-level parallelism (ILP)? Also explain the design challenges of Pipeline processors.

b) Explain the basic concept of CPU machine instruction and its types.

c) Write short-note on Multiport Memory.

d) What is significance of Virtual Memory in advance computer architecture?

e) State the advantages and disadvantages of shared versus memory mapped I/O.

f) How the performance of the processors is improved by using the Superscalar architectures?

g) Explain the types of system performance factors in a parallel architecture.

(7x4)

2.

a) In the pipeline organization, it is difficult to keep a large pipeline at maximum rate because of the pipeline hazards. Explain Control Hazards in pipeline hazards by taking suitable program.

b) Explain the Flynn's classification for Computer Architectures based on the nature of the instruction flow executed by the computer with diagram.

(9+9)

3.

a) Explain the basic terms related to Bus Protocols. Give reason for increasing bus bandwidth of Input/Output devices.

b) Discuss the limitation factor of parallel execution by taking simple example.

(9+9)

4.

a) What is a pipeline bubble? Deduce what is in a pipeline stage that is "executing" a bubble?

b) What are the properties of the Vector Processors? Explain each component of Vector-Register Processors with diagram.

(8+10)

5.

a) What is the need of VLIW architecture? Also compare its properties with Explicitly Parallel Instruction Computing (EPIC) model.

b) In Program parallelism, what are the different issues of scheduling?

c) How Cache memory performance is analyzed in advance processor architecture.

(6+5+7)

6.

a) Give classification criteria for interconnection networks (INs).

b) Explain Multiple-Instruction Multiple-Data streams (MIMD) parallel architectures model with diagram.

(8+10)

7.

a) State network properties with respect to system architectures. Explain Dynamic Networks Bus Systems in detail.

b) Vectorizing compilers generally detect loops that can be executed on a pipelined vector computer. Are the vectorization algorithms used by vectorizing compilers suitable for MIMD machine parallelization?

c) What is meant by Cache-Coherency? Explain with the help of a suitable example.

(6+6+6)