S.E.(Cmpn & I.T.) sem 3 (Rev.)
Digital Logic Design & Application 15/12/07

Con. 5133-07. CD-6712

(REVISED COURSE)

(3 Hours) [Total Marks : 100

N.B. (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of the remaining **six** questions.
(3) Assume suitable **additional** data if **required**.

1. (a) Fill in the blanks :— 5

(i) A number in any number system can be represented by the following equation _____ _____ _____ .

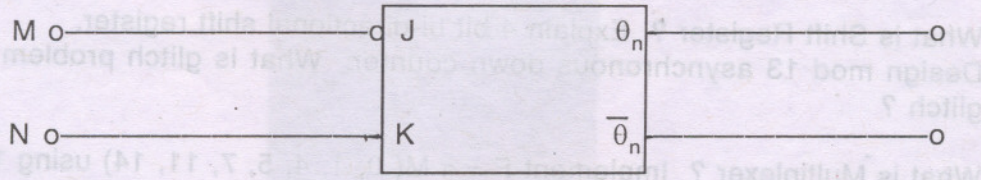
(ii) The excess 3 code is _____ _____ .

(iii) While adding two BCD numbers, if the sum gives an invalid BCD code, then to make it valid _____ _____ .

(iv) Two's complement of a numer is _____ _____ .

(v) Eight bits make a _____ and four bits make a _____ .

(b) Consider the MN FF as shown. Obtain its characteristic table, characteristic equation and excitation table. 5



(c) Carry out following arithmatic without converting to any other base. 4

(i) $(B\ 6\ A)_{16}$ $-(2\ F\ E)_{16}$

(ii) $(7\ 5\ 6)_9$ $\times (5\ 3)_9$

(d) A seven bit Hamming Code is received as 1000010. Correct it for any errors. Why Hamming Code is called as error correcting code ? Justify. 4

(e) Subtract $(365)_8$ from $(173)_8$. Use 8's complement addition to perform subtraction. 2

2. (a) Simplify using Boolean Theorems and implement using AOI gates only. 10

(i) $\overline{\left[(C+\overline{C}D)(C+\overline{C}\,\overline{D})\right]\left[(AB+\overline{A}\,\overline{B})+(A\oplus B)\right]}$

(ii) $\overline{AB+\overline{A}\,\overline{B}+(A+B)\cdot(\overline{A}+B)}$

(b) Given the logical expression—

$$Y=(A+B+\overline{C}+\overline{D}).(\overline{A}+C+\overline{D})\cdot(\overline{B}+C)(\overline{B}+\overline{C})\cdot(A+\overline{B})(\overline{B}+\overline{D})$$

(i) Express in std POS form 3
(ii) Draw K map for the equation. 3
(iii) Minimize and realise using NOR gates only. 4

3. (a) Realise FULL Subtractor circuit using 4 : 1 Multiplexer and 3L : 8L Decoder. 10
[Active high I/p and Active low O/p decoder]
(b) Using Quine McCluskey Method, determine the minimal SOP form for : 10
$F(A, B, C, D, E, F, G) = \Sigma m$ (20, 28, 38, 39, 52, 60, 102, 103, 127)

4. (a) The Computer Engineering Society wishes to select members on its board of Governers. 10
The following criterias are applied. The candidate should be a member of the society for a minimum period of 12 years. A male candidate should have a professional experience of 20 years or more. A female candidate will be eligible if she has an experience of 15 years. Design and implement the above circuit.
(b) Design and implement two 2 bit multiplier circuit. 10

5. (a) For synchronous sequence counter with sequence 2 — 6 — 5 — 3 — 1— 0 — 2
(i) Give present state/next state table 2
(ii) Write state transition table using D flip-flops. 3
(iii) Simplify and realize the circuit. Draw state diagram. 5
(iv) If the counter enters any unused state will it go to lockout condition. Justify. 2
(b) Draw neat diagram of two I/p TTL NAND gate and explain its operation. 8

6. (a) What is Shift Register ? Explain 4 bit bi-directional shift register. 10
(b) Design mod 13 asynchronous down counter. What is glitch problem ? How to avoid glitch ? 10

7. (a) What is Multiplexer ? Implement $F = \pi M(0, 1, 4, 5, 7, 11, 14)$ using 16 : 1 multiplexer. 8
(b) Write short notes on [any **two**] 12
(i) Master slave JK flip-flop
(ii) 74180 parity generator and checker
(iii) PAL and PLA.