S.E. (comp) sem III (R) Digital Logic Design & Application

Con. 2721-09.

## (3 Hours)

(REVISED COURSE)

[Total Marks : 100

25-05-09

3 pm to 6pm

6

6

4

4

- N.B.: (1) Question No. 1 is compulsory.
  - (2) Attempt any four questions out of remaining six questions.
- 1. (a) Convert (670.17)<sub>8</sub> into decimal, binary and hex.
  - (b) Design 16: 1 MUX using 4: 1 MUX.
  - (c) Design a full subtractor using only NAND gates.
  - (d) Simplify the following using Boolean Laws :
    - (i)  $A + \overline{A} B + \overline{A} \overline{B} C + \overline{A} \overline{B} \overline{C} D$
    - (ii)  $A \left[ B + C \overline{(AB + AC)} \right]$
- 2. (a) Simplify using K-map, obtain SOP equation and realize using only NAND gates. **10**  $f(A, B, C, D) = \pi M(1, 2, 3, 8, 9, 10, 11, 14) + d(7, 15).$ 
  - (b) Consider a chemical mixing tank for which there are 3 variables of interest : 10 liquid level, pressure and temperature. The alarm will be triggered under the following conditions :
    - (i) Low level with high pressure
    - (ii) High level with low pressure
    - (iii) High level with low temperature and high pressure.

Design the system, implement using only NOR gates.

- 3. (a) Design BCD to 7-segment code converter.
  (b) Draw the 2-input TTL NAND gate and explain. List important characteristics 10 of TTL family.
  4. (a) Design a BCD adder using 4-bit binary adders and explain.
  (b) Design a MOD-6 synchronous up-counter and explain its operation.
  10
- 5. (a) Simplify using K-map and realize using NOR gates. 10  $f(A, B, C, D) = \Sigma m(1, 3, 7, 11, 15) + d(0, 2, 5, 8, 14).$ 
  - (b) Draw a 4-bit Johnson counter using shift register and prove that it is "Divide 10 by 4" logic.
- 6. (a) Simplify using Quine McClusky method.10 $f(A, B, C, D) = \pi m(0, 2, 3, 6, 7, 8, 9, 12, 13).$ <br/>Realize the equation using any universal gate.10(b) Implement the following expression using 8 : 1 MUX.10

 $f(A, B, C, D) = \Sigma m(0, 1, 5, 7, 9, 10, 15).$ 

Write short notes on :-DeMorgan's Theorems (a) (b) NOR as universal gate (c)ALU (d) TTL Vs CMOS logic family. 20