(a) Prove that the mid band voltage gain falls by $1/\sqrt{2}$ at the lower cut-off frequency. Hence **20**
obtain the expression for that.

(b) For what type of a load, 'L' filler and 'C' filter is used ?
Also write the significance of bleeder resistance in LC filter.

(c) Give the device characteristics. Determine V_C, R_B and R_C for the following fixed
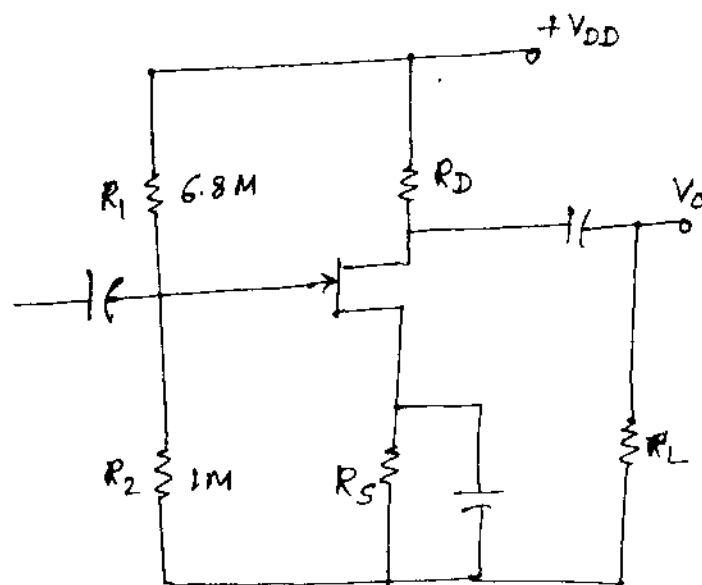biased configuraion.
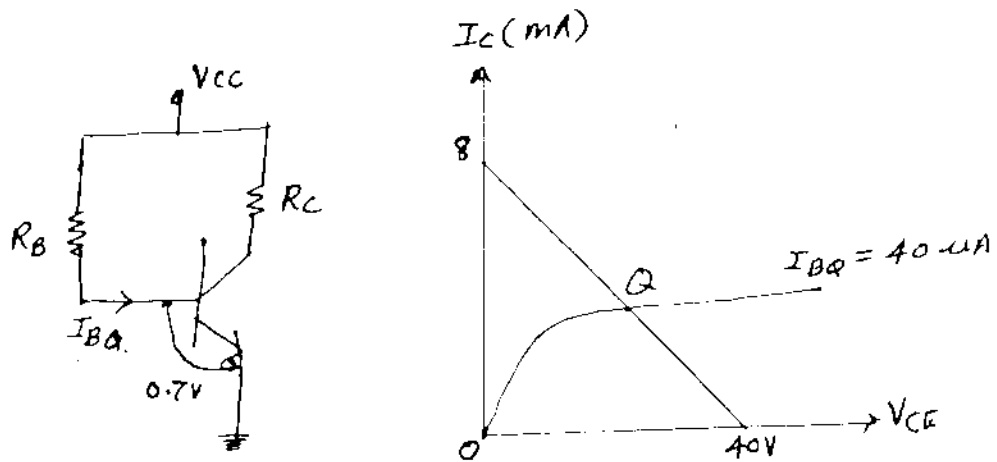
(d) Condition for 'zero temp. drift' in FET. Explain.
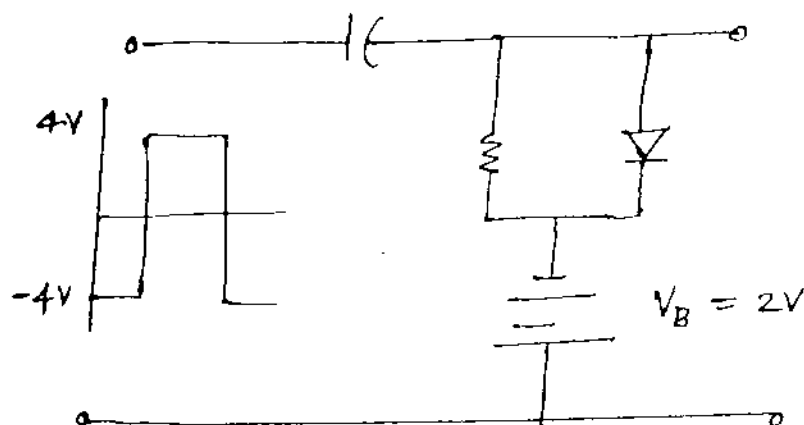
(a) Determine the co-ordinates of Q Point. **10**
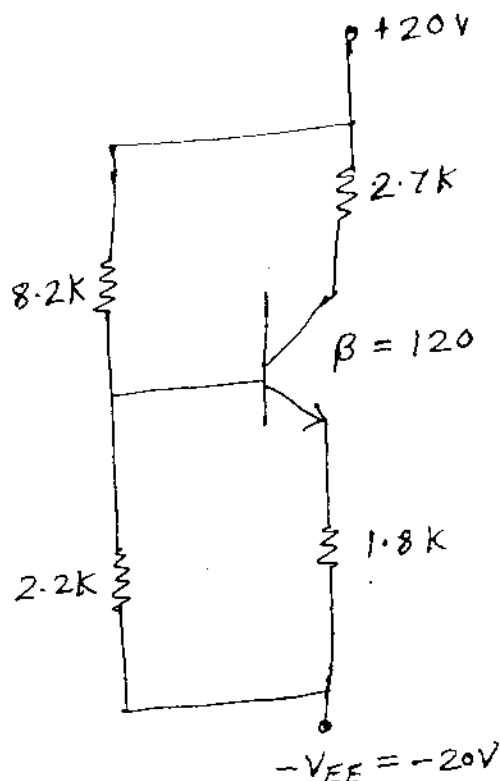
(b) For the circuit shown below, determine A_V, Z_i and Z_o

$V_{DD} = 20$ V $I_{DSS} = 10$ mA
$R_D = 1.5$ k $V_p = 3$ V
$R_s = 1$ k $r_d = 50$ k
$R_L = 10$ k $I_{DQ} = 3.8$ mA

3. (a) Design a single stage RC coupled amplifier for the following specifications—
gain $= 10$, $f_L = 20$ Hz, $V_0 = 2.5$ V
   (b) Draw o/p waveform for,

$V_B = 2V$

4. (a) Draw various biasing schemes used for BJTs.
   (b) Draw a neat diagram with proper biasing of JFET CG amplifier. Derive expressions voltage gain, input impedance and o/p impedance.

5. Design a single stage RC coupled CE amplifier using transistor for the following specificat

$$|A_V| \geq 100, \qquad f_L = 20 \text{ Hz}, \qquad V_{cc} = 20 \text{ V}, \qquad S < 10.$$

a) The differential amplifier circuit is shown in the **figure** biased at $IQ = 0.5$ mA. The transistor 20
parameters are $\beta = 150$, $V_{A_1} = V_{A_2} = 125$ V and $V_{A_3} = V_{A_4} = 85$ V.

Draw equivalent circuit of BJT differential amplifier with active load.
b) Determine the open circuit differential mode voltage gain.
c) Find the differential mode voltage gain with $R_L = 100$ k.
d) Find the o/p resistance looking back from the load R_L.
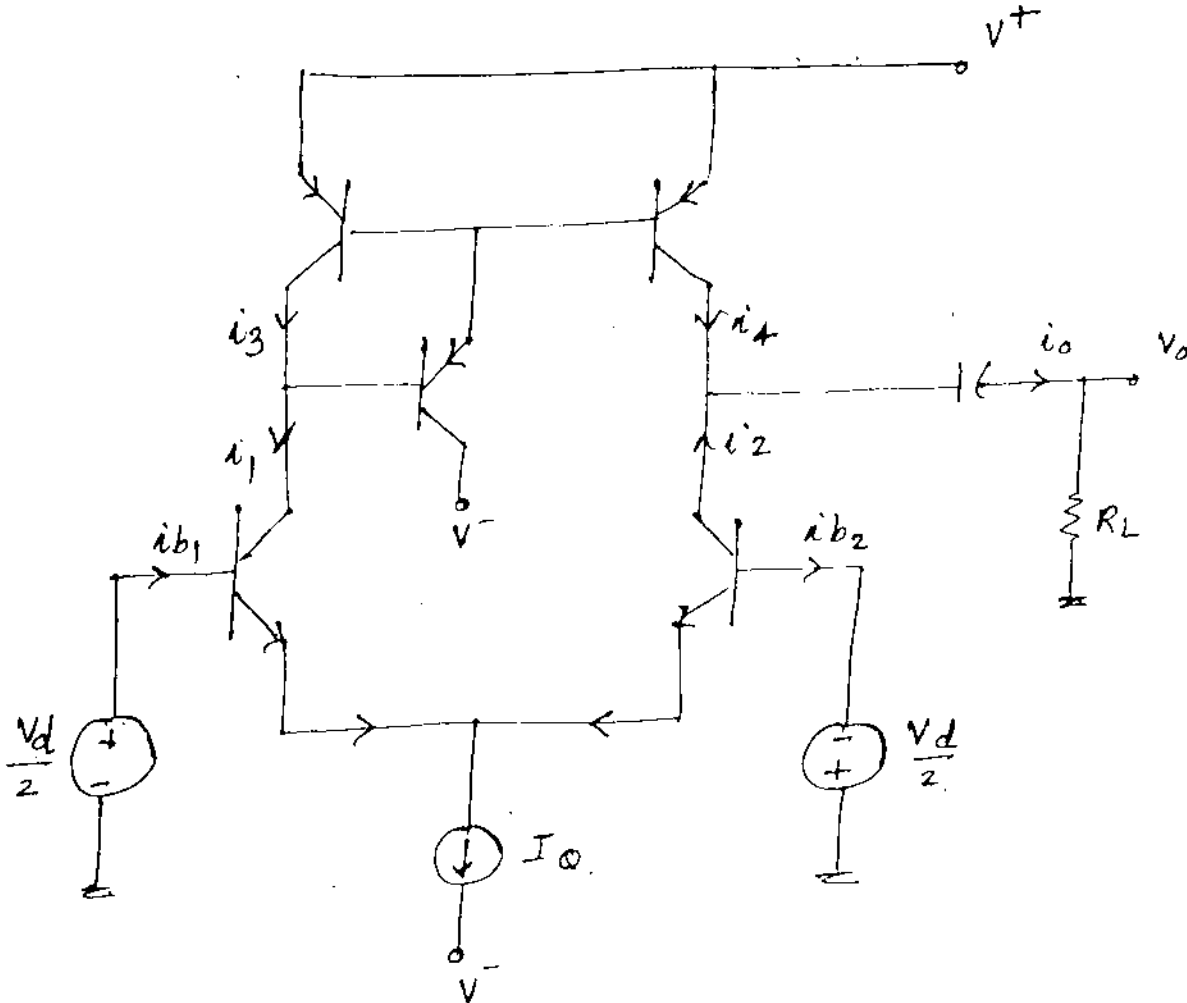
Write short notes on any **four** :— 20
  (a) Cascode amplifier
  (b) Short circuit and open circuit time constants
  (c) High frequency model of BJT and FET
  (d) LED
  (e) VMOS.

(Refer Page No. 4 for DATA SHEET)

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