

AMIETE – CS/IT (OLD SCHEME)

Code: AC07 / AT07

Time: 3 Hours

Subject: COMPUTER ARCHITECTURE

Max. Marks: 100

JUNE 2011

NOTE: There are 9 Questions in all.

- Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.
- The answer sheet for the Q.1 will be collected by the invigilator after 45 Minutes of the commencement of the examination.
- Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.
- Any required data not explicitly given, may be suitably assumed and stated.

Q.1 Choose the correct or the best alternative in the following: (2 × 10)

- a. Which of the following fields must occur explicitly as a part of machine instruction?
- (A) Operation Code (B) Source operand reference
(C) Result operand reference (D) Next instruction reference
- b. Which of the following is not a feature of RISC architecture?
- (A) Large number of registers
(B) Pipelining
(C) Instruction set close to a high-level language
(D) Simple instruction format
- c. Which of the following is an advantage of *interrupt-driven I/O* over *programmed I/O*?
- (A) Faster completion of the data transfer
(B) Higher bandwidth availability
(C) Better CPU utilization
(D) Smaller memory requirement
- d. An interrupt in which the external device supplies its address as well as the interrupt request is
- (A) Vectored interrupt (B) Mask able
(C) Polled (D) Non mask able
- e. Suppose the cache and main memory access times are 100 ns and 1200 ns respectively. The cache is used for paging and the hit ratio of finding the page table entry in the cache is 98%, what is the effective paged memory access time?
- (A) 240 ns (B) 220 ns
(C) 250 ns (D) 1200 ns

- f. The base 10 number 65535 is represented in hexadecimal as...?
- (A) 0×FFFFF (B) 0×FFFF
(C) 0×FFF (D) 0×FFFFFF
- g. To obtain better memory utilization dynamic loading is used. For implementing it,
- (A) Special support from the hardware is required
(B) Special support from the Operating System is required.
(C) Special support from the OS and Hardware both are required.
(D) None of the above.
- h. What does the UART chip do?
- (A) Converts analog data to digital data and digital data to analog data.
(B) Converts parallel data to serial data and serial data to parallel data.
(C) Converts parallel data to serial data and analog data to digital data
(D) Converts serial data to parallel data and digital data to analog data.
- i. The technique whereby part of the program is stored on disk and is brought into memory for execution as needed is called
- (A) Memory allocation (B) Virtual storage
(C) Interrupts (D) Prioritized memory
- j. The Boolean function $x'y' + xy + x'y$ is
- (A) $x' + y'$ (B) $x + y$
(C) $x + y'$ (D) $x' + y$

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

- Q.2** a. Write briefly about computer fundamental system. Explain memory unit functions. Explain the meaning of memory locations and addresses. (6)
- b. Find out the simplified equation for the function f (a, b, c) using sum of products from the following truth table. Also show the design of the circuit using only NAND gates. (6)

A	B	C	D
0	0	0	1
0	1	0	1
0	1	0	0
0	0	1	0
1	0	1	0
1	1	0	0
1	1	1	1

- c. What is the role of compiler in program execution? (4)

- Q.3** a. Compare the features of combinational circuits and sequential circuits. Give their applications. (6)
- b. What are the steps involved in programmed input/output? Explain the situations in which you would prefer Programmed input/output over interrupt driven input/output. (4)
- c. Explain the construction of D Flip Flop from SR flip flop. (6)
- Q.4** a. Formulate a mapping procedure that provides eight consecutive microinstructions for each sub-routine. The operation code has six bits and control memory has 2048 words. (4)
- b. What are the functions of a typical Input / Output Interface? (6)
- c. Show step by step multiplication process using Booth algorithm when the following binary numbers are multiplied. Assume 5-bit register hold signed number. The multiplicand is +25. i.e., $(+25) \times (+13)$ (6)
- Q.5** a. Explain Daisy-Chain priority interrupt. (4)
- b. Explain horizontal and vertical formats used in microprogrammed control unit. Give an example for each. (6)
- c. Explain any one of the following asynchronous data transfer for source-initiated and destination initiated data transfer
 (i) Strobe control
 (ii) Handshaking control (6)
- Q.6** a. Draw the flow chart of instruction fetch cycle. (4)
- b. Explain address sequencing involved in microprogrammed control unit. Give the block diagram. (8)
- c. Explain the DMA driven Data transfer technique. (4)
- Q.7** a. What is baud rate? Consider a serial transmission whose transfer rate is 9 characters per second. The system uses 2 stop bits and has eight signaling states. Calculate its baud rate. (4)
- b. Write an assembly program to reverse a given string. (6)
- c. Explain the following addressing modes with one example each. Also give one use of each addressing mode (6)
 (i) Register addressing
 (ii) Index addressing
 (iii) Stack addressing
- Q.8** a. Draw and explain the block diagram of 4-bit adder subtractor circuit using full adders. (5)
- b. A computer has 32 registers, ALU has 64 operations. All are connected to a common bus system. Formulate a control word for the computer, specify and explain the bits in each field of control word. (8)

- c. Show the bit configuration of 24-bit register that hold the number equivalent to $(215)_{10}$ in
- (i) binary coded octal
 - (ii) binary coded hexadecimal
 - (iii) BCD
- (3)**

- Q.9** a. Consider a virtual memory system with the following properties:
44-bit virtual byte address
4 KB pages
28 bit physical byte address
What is the total size of the page table measured in bits for a process using this virtual memory system? (You may assume that disk addresses are not stored in the page table.) **(8)**
- b. What's the difference between Write-Through and Write-Back Caches? Explain advantages and disadvantages of each. **(4)**
- c. Cache Size is 128KB, Block size is 64B and the cache is Two-Way Set Associative. For a 64-bit physical address, give the division between Block Offset, Index and Tag. **(4)**