**Code: AC07/AT07** **Subject: COMPUTER ARCHITECTURE**
**Time: 3 Hours** **Max. Marks: 100**

DECEMBER 2008

**NOTE: There are 9 Questions in all.**

- **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

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**Q.1 Choose the correct or best alternative in the following: (2x10)**

a. PAL circuit consists of

**(A)** Fixed OR & programmable AND logic
**(B)** Programmable OR & Fixed AND Logic
**(C)** Fixed OR & fixed AND logic
**(D)** Programmable OR & programmable AND logic

b. 8085 microprocessor carryout the subtraction by

**(A)** BCD subtraction method
**(B)** Hexadecimal subtraction method
**(C)** 2's complement method
**(D)** Floating Point subtraction method

c. CPU checks for an interrupt signal during

**(A)** Starting of last Machine cycle
**(B)** Last T-State of instruction cycle
**(C)** First T-State of interrupt cycle
**(D)** Fetch cycle

d. During DMA acknowledgement cycle, CPU relinquishes

**(A)** Address bus only **(B)** Address bus & control bus
**(C)** Control bus & data bus **(D)** Data bus & address bus

e. If the clock input applied to a cascaded Mod-6 & Mod-4 counter is 48KHz. Than the output of the cascaded arrangement shall be of

**(A)** 4.8 KHz **(B)** 12 KHz
**(C)** 2 KHz **(D)** 8 KHz

f. If the stack pointer is initialised with $(4FEB)_H$, then after execution of Push operation in 8085 microprocessor, the Stack Pointer shall be

**(A)** 4FEA **(B)** 4FEC
**(C)** 4FE9 **(D)** 4FED

g. A more efficient way to organise a Page Table is by means of an associative memory having

**(A)** Number of words equal to number of pages
**(B)** Number of words more than the number of pages
**(C)** Number of words less than the number of pages
**(D)** Any of the above

h. If there are four ROM ICs of 8K and two RAM ICs of 4K words, than the address range of Ist RAM is (Assume initial addresses correspond to ROMs)

**(A)** $(8000)_H$ to $(9FFF)_H$ **(B)** $(6000)_H$ to $(7FFF)_H$
**(C)** $(8000)_H$ to $(8FFF)_H$ **(D)** $(9000)_H$ to $(9FFF)_H$

i. $A \oplus B \oplus C \odot$ equal to A B C for

**(A)** A=0, B=1, C=0 **(B)** A=1, B=0, C=1
**(C)** A=1, B=1, C=1 **(D)** All of the above

j. Gray code equivalent of $(1000)_2$ is

**(A)** $(1111)_G$ **(B)** $(1100)_G$
**(C)** $(1000)_G$ **(D)** None of these

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**Answer any FIVE Questions out of EIGHT Questions.**
**Each question carries 16 marks.**

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**Q.2** a. Discuss the main features of associative memory Page Table. How does it work in mapping the virtual address into Physical memory address? **(7)**

b. A Virtual memory has a Page Size of 1K words. There are eight Pages and four blocks. The associative memory page table contains the following entries.

| Page | Block |
|---|---|
| 6 | 0 |
| 1 | 1 |
| 4 | 2 |
| 0 | 3 |

Give the list of virtual addresses in decimal that will cause a Page fault if used by CPU. **(6)**

c. How LRU technique is implemented ? **(3)**

**Q.3** a. With neat block diagram explain DMA technique for data transfer. **(7)**

b. State the difference between I/O mapped I/O & Memory mapped I/O. **(6)**

c. What is cycle stealing DMA operation? **(3)**

**Q.4** a. What do you understand by the term micro-operation. Explain Register and Arithmetic types of micro-operation. Show the hardware realization of decrement micro-operation.
i.e. $T1: X \leftarrow X - 1$ **(6)**

b. Implement the following RTL code using common bus and tri-state buffers.
$i: M \leftarrow A$
$j: A \leftarrow Y$
$k: R \leftarrow M$
$l: Y \leftarrow R,\ M \leftarrow R$
Assume M, A, R and Y are to be one bit D Flip-Flop. **(6)**

c. A Register 'A' holds on 8-bit binary number 11011001. Determine the operand 'B' and the logic micro-operation to be performed in order to change the value of 'A' to
(i) 01101101
(ii) 11111101 **(4)**

**Q.5** a. Give the flow chart of division of two signed magnitude data. Discuss the logic of the flow chart. **(10)**

b. Give the flow chart for multiplication of two Signed magnitude numbers. Illustrate with the example of multiplying (–3) with (+4). **(6)**

**Q.6** a. Discuss the operation carried out in a 'subroutine call' instruction. What is the difference between a subroutine and a Macro? Explain recursive subroutine.
**(6+3+3)**

b. Convert the following arithmetic expression from reverse polish notation to infix notation:
ABXYZ+*–/
Write a program using three address instruction to evaluate the same. **(4)**

**Q.7** a. What are the interrupts? Explain different types of interrupts. **(8)**

b. What do you mean by Fetch cycle, Instruction cycle, machine cycle and Interrupt acknowledgement cycle. **(4)**

c. Explain the significance of different fields of an instruction with an example. **(4)**

**Q.8** a. The 8-bit registers A, B, C & D are loaded with the value $(F2)_H$, $(FF)_H$, $(B9)_H$ and $(EA)_H$ respectively.

Determine the register content after the execution of the following sequence of micro-operations sequentially.

(i) $A \leftarrow A + B$, $C \leftarrow C + Shl(D)$

(ii) $C \leftarrow C \wedge D$, $B \leftarrow B + 1$.

(iii) $A \leftarrow A - C$.

(iv) $A \leftarrow Shr(B) \oplus Cir(D)$ **(8)**

b. Using 4 bit ring counter with Parallel load and a 4-bit adder, draw the block diagram for implementing following RTLs,

$P : R_1 \leftarrow R_1 + R_2$

$P'Q : R_1 \leftarrow R_1 + 1$

where $R_1$ is a counter with Parallel load and $R_2$ is a 4-bit register.

**(8)**

**Q.9** a. Design a synchronous self starting counter using S-R flip flops for counter the sequence 0, 2, 3, 5, 8, 7, 15, 12, 11, 10 & repeat. **(8)**

b. Minimise the logic expression $f(d, b, a, c) = \sum m(1, 3, 5, 6, 7, 11, 13, 14)$ and don't care for $M_4$, $M_9$, $M_{10}$. Realise the simplified boolean expression by using NOR gates only. **(8)**