ENGINEERING & MANAGEMENT EXAMINATIONS, JUNE - 2007

COMPUTER ARCHITECTURE & ORGANIZATION

SEMESTER - 4

Time : 3 Hours] [Full Marks : 70

GROUP - A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : $10 \times 1 = 10$

i) With 2's complement representation, the range of values that can be represented on the data bus of an 8 bit microprocessor is given by

a) - 128 to + 127 b) - 128 to + 128

c) - 127 to + 128 d) - 256 to + 128. ☐

ii) Booth's algorithm for computer arithmetic is used for

a) multiplication of number in sign magnitude form

b) multiplication of number in 2's complement form

c) division of number in sign magnitude form

d) division of number in 2's complement form. ☐

iii) Micro instructions are kept in

a) Main memory b) Control store

c) Cache d) none of these. ☐

iv) What is the 2's complement representation of - 24 in a 16-bit microcomputer ?

a) 0000 0000 0001 1000 b) 1111 1111 1110 1000

c) 1111 1111 1110 0111 d) 0001 0001 1111 0011. ☐

v) Associative memory is a

a) Pointer addressable memory b) Very cheap memory

c) Content addressable memory d) Slow memory. ☐

vi) The principle of locality justifies the use of

a) Interrupts b) Polling

c) DMA d) Cache Memory. ☐

vii) In a microprocessor the address of the next instruction to be executed is stored in

a) stack pointer b) address latch

c) program counter d) general purpose register. ☐

viii) A system has 48 bit virtual address, 36 bit physical address and 128 MB main memory; how many virtual and physical pages can the address spaces support ?

a) $2^{36}, 2^{24}$ b) $2^{12}, 2^{36}$

c) $2^{24}, 2^{34}$ d) $2^{34}, 2^{36}$. ☐

ix) The basic principle of the von Neumann computer is

a) storing program and data in separate memory

b) using pipeline concept

c) storing both program and data in the same memory

d) using a large number of registers. ☐

x) Physical memory, broken down into groups of equal size, is called

a) Page b) Tag

c) Block d) Index. ☐

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. $3 \times 5 = 15$

2. What is virtual memory ? Why is it called virtual ? Write the advantage of virtual memory.

3. What is meant by parallel processing ? What is the basic objective of parallel processing ?

4. What do you mean by instruction cycle, machine cycle and *T* states ?

5. Distinguish between vectored interrupt and non-vectored interrupt.

6. Compare RISC with CISC.

GROUP – C

(Long Answer Type Questions)

Answer any *three* questions. $3 \times 15 = 45$

7. a) What is pipelining ?

   b) What are speedup, throughput and efficiency of a pipelined architecture ?

   c) Describe pipeline hazards.

   d) Compare between centralized and distributed architecture. Which is the best architecture among them and why ? $2 + 3 + 5 + 3 + 2$

8. a) What is meant by DMA ? Why is it useful ? Briefly explain with suitable diagram, the DMA operation in association with CPU.

   b) Draw the schematic diagram for daisy chain polling arrangement in case of vectored interrupt for three devices. $2 + 2 + 6 + 5$

9. a) Discuss the principle of carry look ahead adder and design a 4-bit CLA adder and estimate the speed enhancement with respect to ripple carry adder.

   b) Briefly state the relative advantages and disadvantages of parallel adder over serial adder.

   c) $X = (A + B) XC$

   Write down the zero address, one address, three address instructions for the expression. $4 + 3 + 2 + 6$

10. a) Why do we require memory hierarchy ? Show the memory hierarchy diagram indicating the speed and cost.

b) Distinguish between SRAM and DRAM.

c) How many 256X4 RAM chips are needed to provide a memory capacity of 2048 bytes ? Show also the corresponding interconnection diagram.

d) A disk drive has 20 sectors / track, 4000 bytes / sector, 8 surfaces all together. Outer diameter of the disk is 12 cm and inner diameter is 4 cm. Inter-track space is 0.1 mm. What is the no. of tracks, storage capacity of the disk drive and data transfer will be there from each surface ? The disk rotates at 3600 rpm. (2 + 1) + 3 + (2 + 2) + 5

11. a) Explain Booth's Algorithm. Apply Booth's algorithm to multiply the two numbers $(+ 14)_{10}$ and $(- 12)_{10}$. Assume the multiplier and multiplicand to be of 5 bits each.

b) Give the flowchart for division of two binary numbers and explain. 10 + 5