SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E - EEE
Title of the paper: Integrated Circuits
Semester: V — Max. Marks: 80
Sub.Code: 414502 — Time: 3 Hours
Date: 08-11-2008 — Session: FN

PART – A (10 x 2 = 20)

Answer All the Questions

1. Classify the ICs on the basis of device used.

2. Mention the advantages of ion implantation.

3. List any four manufacturers of linear ICs with their codes.

4. Define slew rate.

5. What is a precision diode?

6. What is a log amplifier?

7. Discuss the disadvantages of passive filter

8. What is a Sallen-Key filter?

9. List the applications of PLL.

10. Define Capture range.

PART – B (5 x 12 = 60)

Answer All the Questions

11. (a) Discuss the various ways for fabricating p-n-p transistor.(8)
(b) What is meant by parasitic capacitance? Explain. (4)

(or)

12. Describe the diffusion process

13. Explain how a current mirror can be an active load for difference amplifier to obtain a very large voltage gain.

(or)

14. Explain in detail about the frequency compensation methods.

15. (a) What is an instrumentation amplifier? Explain its working and applications with suitable diagram.
(b) Draw and explain the clipper which will clip the input signal below a reference voltage.

(or)

16. Draw and explain the circuit of a voltage to current if the load is
(a) floating and
(b) grounded. Is there any limitation on the size of the load when grounded.

17. (a) Define Bessel, Butterworth and chebyshev filters. Also compare them with their response. (5)
(b) Draw and explain the narrow band filter and derive the relation for output, bandwidth and Q factor. (7)

(or)

18. Draw and explain the circuit of mono-stable multi-vibrator using op-Amp. Also derive the expression for time delay.

19. (a) Write short notes on VCO.
(b) Explain how successive approximation ADC performs the conversion with the help of its functional diagram.

(or)

20. Using a neat circuit diagram, explain how 565 PLL can be used as a FSK demodulator.