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SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act,1956)

Course & Branch :B.E - EEE
Title of the Paper :Integrated Circuits — Max. Marks :80
Sub. Code :414502 — Time : 3 Hours
Date :11/11/2009 — Session :FN

PART - A (10 x 2 = 20)

Answer ALL the Questions

1. Classify ICs on the basis of chip complexity.
2. Mention any two advantages of integrated circuits over discrete component circuit.
3. Define the term “slew rate”
4. Draw the equivalent circuit of a practical Op-amp.
5. What is an instrumentation amplifier?
6. Define common mode rejection ratio of an OPAMP.
7. What is the purpose of a Schmitt trigger?
8. Why are active filters preferred?
9. List the applications of Phase-Locked Loops (PLL).
10. List the various A/D conversion techniques.

PART – B (5 x 12 = 60)

Answer All the Questions

11. Explain the word “Epitaxy” and describe the Epiraxial growth process.

(or)

12. Discuss various methods used for fabricating IC resistors and compare their performance.

13. List and explain the parameters given in manufacture's data-sheet of an OPAMP.

(or)

14. (a) What is the difference between the open loop and closed loop gain of an Op-amp? (4)

    (b) An OPAMP has a slew rate of $2V/\mu_5$; Find the rise time for an output voltage of 10V amplitude resulting from a rectangular pulse input if the Op-amp is slew rate limited. (8)

15. Draw the circuit of a voltage to current converter if the load is
    (a) floating and
    (b) grounded. Is there any limitation on the size of the load when grounded?

(or)

16. Write short notes on:
    (a) Sample and Hold circuits.
    (b) Precision Rectifiers.

17. (a) Design a HPF at a cut-off frequency of 1 KHZ and a pass band gain of 2. (4)

    (b) Describe the circuit and operation of a switched capacitor low pass filter. (8)

(or)

18. (a) Draw the circuit of a Schmitt trigger using 555 timer and explain its operation.

    (b) Design a monostable multivibrator using 555 timer to produce a pulse width of 100ms.

19. With a neat block diagram explain the operation of a Phase-Locked Loop (PLL)

(or)

20. Classify DACs on the basis of their output and name the essential parts of a DAC. Also, explain the operation of Dual – Slope ADC.