[3762]-203

S.E. (Comp.) (First Semester) EXAMINATION, 2010

DIGITAL ELECTRONICS AND LOGIC DESIGN

(2008 COURSE)

Time : Three Hours   **Maximum Marks : 100**

N.B. :—(i) Answer Q. No. **1** *or* **2**, Q. No. **3** *or* **4**, Q. No. **5** *or* **6** from Section I and answer Q No. **7** *or* **8**, Q. No. **9** *or* **10**, Q. No. **11** *or* **12** from Section II.

(ii) Answers to the two Sections should be written in separate answer-books.

(iii) Neat diagrams must be drawn wherever necessary.

(iv) Figures to the right indicate full marks.

(v) Assume suitable data if necessary.

SECTION I

1. (a) Convert the following octal numbers into its equivalent decimal and hex. :   [6]

   (i) $(555)_{octal}$

   (ii) $(777)_{octal}$

   (b) Solve the following equations using corresponding minimization techniques, also draw MSI design for the minimized output equation :

   (i) $Z = f(A, B, C, D) = \pi(2, 7, 8, 10, 11, 13, 15)$

   (ii) $Z = f(A, B, C, D) = \sum(0, 3, 4, 9, 10, 12, 14)$. [12]

2. (a) Express the following numbers in binary, show the step-by-step equations and calculations ?

   (i) $(110.110)_{Decimal}$

   (ii) $(234.234)_{Decimal}$ [6]

   (b) Convert 4-bit grey code into corresponding BCD code. Show truth table and MSI circuit.   [6]

   (c) Perform the following hex-decimal substraction and show the answer in hex-decimal only :   [6]

   (i) $(ABC)_{Hex} - (CBA)_{Hex}$

   (ii) $(759)_{Hex} - (957)_{Hex}$

3. (a) With the help of Quine-McClusky technique determine the PI, EPI for the following equation :   [10]

   $$Z = f(A, B, C, D) = \Sigma\ (0,\ 3,\ 8,\ 9,\ 10,\ 12,\ 15)$$

   (b) Explain standard TTL characteristics in brief.   [6]

Or

4. (a) Draw z-i/p standard TTL NAND gate with totem pole. Explain operation of transistor (ON/OFF) with suitable input conditions and truth table.   [10]

   (b) What is logic family ? Explain types of logic families in detail. [6]

5. (a) Draw and explain 4-bit BCD adder using IC 7483. Explain any *two* BCD addition operations. [10]

(b) Explain the working of cascaded mode magnitude comparator using IC 7485 ? [8]

Or

6. (a) Explain decoder (1 : 8) as a full adder and full subtractor Show your design. [8]

(b) Design 14 : 1 mux using 4 : 1 mux (with enable inputs). Explain the truth table of your circuit in short. [8]

SECTION II

7. (a) Design SR flip-flop using JK flip-flop. [4]

(b) Explain with a neat diagram working of parallel in serial out 4-bit shift register. Draw necessary timing diagram. [6]

(c) Give any *four* applications of shift registers. Also explain 4-bit Johnson's counter. [8]

Or

8. (a) Explain with a neat diagram working of 3-bit up-down synchronous counter. Draw necessary timing diagram. [10]

(b) Design a sequence generator with a sequence 1101011. [8]

9. (a) With the help of an ASM chart design a modulo 6 up-down counter. [10]

(b) Write VHDL code for 4-bit full adder. [6]

Or

10. (a) Describe architectural blocks of FPCaA. Briefly explain function of each. [10]

(b) Write VHDL code for 4 : 1 MUX. [6]

11. (a) Design using PLD a 3 : 8 decoder. [8]

(b) Draw a generalised block diagram of a microprocessor. Briefly explain function of each block. [8]

Or

12. (a) Using PLDs design a 4-bit Gray code counter. [8]

(b) Explain, what is a bus ? Give different types of bus used by a microprocessor. [4]

(c) Explain the function of :

(1) ALU

(2) Program counter

(3) Instruction register. [4]