S.E. Sem 3 (Rev.) Comp. Digital Logic Design and Application. 17/12/08

ws Oct 08 247

Con. 5677–08. (REVISED COURSE) RC–8922

(3 Hours) [Total Marks : 100

N.B. : (1) Question No. **1** is **compulsory**.
(2) Attempt any **four** questions out of remaining **six** questions.
(3) Assume **suitable** data and state it **clearly**.

1. (a) Convert $(157{\cdot}63)_8$ into decimal, binary and hexadecimal system. 4
   (b) Simplify using boolean laws : 4

$$\overline{\overline{AB} + \overline{A} + AB}$$

   (c) Design full adder using half adders. 4
   (d) State and prove De Morgan's theorem. 4
   (e) Implement the boolean function with NAND – NAND logic 4
   $F(A, B, C) = \Sigma\, m(0, 1, 3, 5)$

2. (a) Using boolean laws, prove NAND and NOR gates as universal gates. 10
   (b) Draw 3-bit binary up-down counter and explain the operation. 10

3. (a) What is race condition ? How it is overcome in Master-slave J-K flip flop ? Explain. 10
   (b) State truth table of 3 bit gray to binary conversion and design using 3 : 8 decoder and additional gates. 10

4. (a) Simplify using K-map, $f(A, B, C, D) = \pi\, M(0, 2, 3, 6, 7, 8, 9, 12, 13)$ Write simplified SOP and POS equations and draw logical diagram using NAND gates only. 10
   (b) Simplify the function using Quine McClusky method. $f(A, B, C, D) = \Sigma\, m(4, 5, 8, 9, 11, 12, 13, 15)$ Draw the logical diagram using NAND gates. 10

5. (a) Draw a 2-input TTL NAND gate and explain its operation. 10
   (b) Simplify $F(P, Q, R, S) = \pi\, M(3, 4, 5, 6, 7, 10, 11, 15)$ and implement using minimum no. of gates. 10

6. (a) Design MOD–6 synchronous counter and explain its operation. 10
   (b) Draw 4 bit universal shift register and explain its operation. 10

7. Write short notes on :– 20
   (a) Multiplexer and demultiplexer
   (b) ALU
   (c) Asynchronous vs synchronous counter
   (d) Octal to binary encoder.
