Con. 5818-09. S.E. (Comp) Sem III (CR) SP-7358

Digital Logic Design & Application

(REVISED COURSE)

17/12/09

(3 Hours) [**Total Marks : 100**

2-30 to 5-30

N.B.:(1) Question No. **1** is **compulsory.**

(2) Attempt any **four** questions out of remaining **six** questions.

1. (a) Convert $(2009 \cdot 12)_{10}$ into octal and hexadecimal. 4
   (b) Design (1:16) demultiplexer using (1:4). 4
   (c) Design a full subtractor using a decoder and additional gates. 4
   (d) Simplify and implement using gates : 4

$$Y = \overline{AB}(B + C) + AB\left(\overline{B + C}\right)$$

   (e) State and prove DeMorgan's theorem. 4

2. (a) Simplify using K-map, obtain POS equation and realize using NOR gates : 10
   $f(A, B, C, D) = \pi M (1, 3, 4, 5, 9, 10, 11) \cdot d(6,8)$.
   (b) Draw a twisted ring counter and prove that it is "Divide by 2 N" circuit, where 'N' is number of Flip Flops. Show necessary timing diagrams. 10

3. (a) Prove NAND as universal gate. 10
   (b) Compare TTL, CMOS and ECL families with respect to basic gate, voltage levels, fan-in, fan-out, propagation delay, power dissipation and noise margin. 10

4. (a) Simplify using Quine McClusky method and realize using any universal Gate : 10
   $F(P, Q, R, S) = \Sigma m(1, 2, 6, 8, 10, 11, 14, 15) + d(5, 9)$.
   (b) Implement the following expression using 8:1 MUX. 10
   $f(A, B, C, D) = \Sigma m(0, 1, 3, 5, 7, 10, 11, 13, 14, 15)$.

5. (a) Design a 3-bit even and odd parity generator. 10
   (b) Design a maximum length sequence generator, to generate the sequence 1101001 and repeat. 10

6. (a) Design a 2-bit digital comparator that accepts inputs A and B and gives three outputs G, E and L. 10
      (i) Output G is active, when A > B.
      (ii) Output E is active, when A = B.
      (iii) Output L is active, when A < B.
   (b) Draw a 4-bit universal shift register and explain. 10

7. Write short notes on the following :— 20
   (a) Totem pole output stage of TTL gate.
   (b) Priority encoder.
   (c) Current and voltage parameters of logic gates.
   (d) Race around condition in J-K Flip-Flop.
