Code: AE09 **Subject: ANALOG & DIGITAL ELECTRONICS**
Time: 3 Hours **Max. Marks: 100**

DECEMBER 2010

NOTE: There are 9 Questions in all.

- **Question 1 is compulsory and carries 20 marks. Answer to Q.1 must be written in the space provided for it in the answer book supplied and nowhere else.**
- **The answer sheet for the Q.1 will be collected by the invigilator after half an hour of the commencement of the examination.**
- **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
- **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1 Choose the correct or the best alternative in the following: (2×10)

a. In a differential amplifier, CMRR can be improved by using an increased

(A) emitter resistance **(B)** collector resistance
(C) source resistance **(D)** power supply voltage

b. Ability of an operational amplifier to provide sufficient differential mode signal but to reject the common mode signal is given by

(A) Closed loop gain
(B) Open loop gain
(C) CMRR.
(D) none of the above.

c. A notch filter is a

(A) Wide band pass filter. **(B)** Narrow band pass filter.
(C) Wide band reject filter. **(D)** Narrow band reject filter

d. The number of comparators required to build an eight-bit simultaneous or flash A/D converter is

(A) 127 **(B)** 63
(C) 255 **(D)** 8

e. A data selector is also called a

(A) De-multiplexer **(B)** Priority encoder
(C) Multiplexer **(D)** Decoder

f. In a 1:16 demultiplexer, the number of control inputs will be

(A) 4 **(B)** 1
(C) 2 **(D)** 16

g. Identify the slowest of the family listed below

(A) LSTTL **(B)** TTL
(C) ECL **(D)** Low Power TTL

h. The number of flip-flops needed to construct a BCD decade counter is

(A) 4 **(B)** 3
(C) 10 **(D)** none of these

i. Size of ROM required to implement a 16:1 multiplexer would be

(A) 512k*2 **(B)** 1M*1
(C) 1M*2 **(D)** 128*6

j. A dynamic RAM consist of

(A) 6 transistors. **(B)** 2 transistors and 2 capacitors
(C) 1 transistors and 1 capacitors. **(D)** 2 capacitors only

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Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Calculate the output voltage in terms of V_1 and V_2 as shown in Fig.1. **(8)**

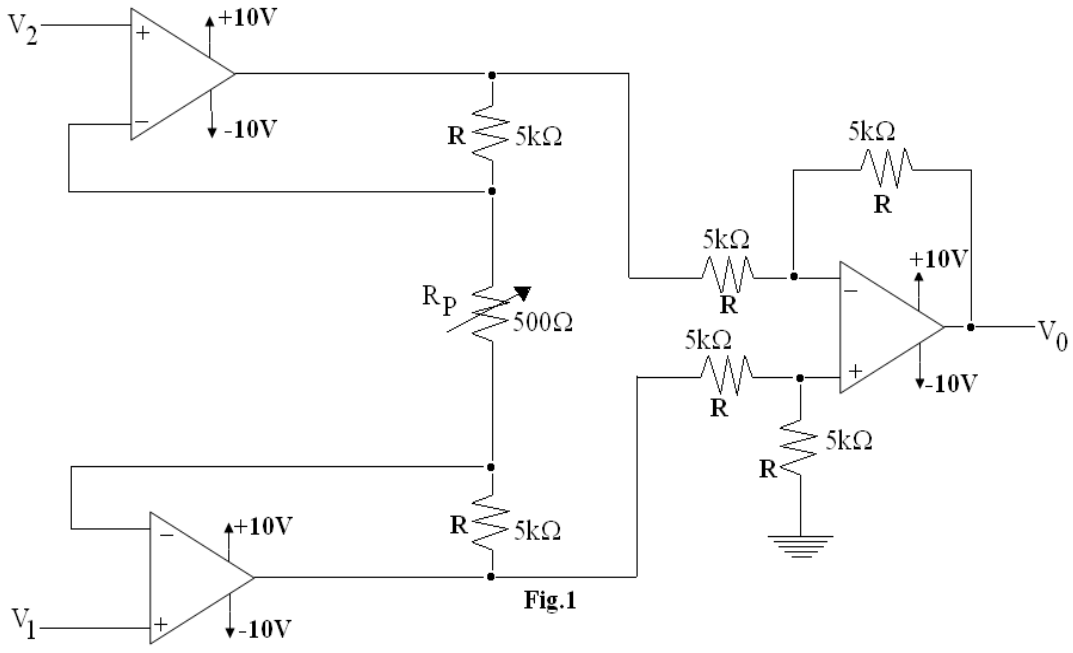

Fig.1

b. Define offset voltage and slew rate of an op-amp. **(4)**

c. In context to frequency compensation, explain internal compensation & external compensation. **(4)**

Q.3 a. Determine the order and 3 dB bandwidth of 1 dB ripple Chebyshev filter that gives a 40 dB attenuation at $\omega/\omega_c = 2$. **(8)**

b. What are Switched-capacitor filters? List the advantages of switched-capacitor filters. **(8)**

Q.4 a. The data sheet of a certain eight-bit A/D converter which have the following specifications:
(i) resolution: eight bits
(ii) full-scale error:0.02%of full scale,
(iii) full scale analogue input:+5V.
Determine the quantization error (in volts) and the total possible error (in volts) **(8)**

b. List the applications of Schmitt trigger circuit. **(4)**

c. What is Schottky diode? Why it is also called hot-carrier diode? How does it differ in construction from a normal p-n junction diode? **(4)**

Q.5 a. Design a two-input NOR and two-input NAND using NMOS logic. **(8)**

b. Explain the working of BJT as an Inverter. **(8)**

Q.6 a. Explain the working of CMOS as an inverter. **(8)**

b. Give general properties of the FETs. **(4)**

c. What is the function of buried layer in the fabrication of Bipolar transistor? **(4)**

Q.7 a. How we interface the TTL-to-ECL family? **(4)**

b. Give the applications of ROM memory. **(4)**

c. Design a 16:1 multiplexer using two 8:1 multiplexer having an active-low ENABLE input. **(8)**

Q.8 a. Design a MOD-10 Johnson counter and also write the count sequence for the same. **(8)**

b. What is the race-around condition and how it can be eliminated? **(8)**

Q.9 a. Describe the serpentine and LARAM organization of a CCD memory. **(8)**

b. A combinational circuit is defined by the functions.
$F_1(A,B,C) = \sum m(3,5,7)$
$F_2(A,B,C) = \sum m(4,5,7)$

Implement the circuit with a PLA having 3 inputs, 3 product terms and 2 outputs. **(8)**