SATHYABAMA UNIVERSITY
(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E - EEE
Title of the paper: Digital Systems
Semester: IV   Max. Marks: 80
Sub.Code: 6C0038   Time: 3 Hours
Date: 05-11-2008   Session: AN

PART – A   (10 x 2 = 20)
Answer All the Questions

1.   Convert the hexadecimal number 68BE to binary number.

2.   State Demorgan's Theorem.

3.   What do you mean by a k-map? Name its advantages and disadvantages.

4.   What do you mean by minterms and maxterms of Boolean expressions?

5.   What is an encoder?

6.   What are the applications of multiplexers?

7.   Realize T flip-flop using J.K flip-flop?

8.   What are the advantages and disadvantages of synchronous over asynchronous counter?

9.   Mention the important characteristics of TTL family.

10.   What are the major draw backs of EEPROM ?

Answer All the Questions

11. Simplify using Quine MeClnsky method
$$F = \Sigma m(0,1,2,3,4,7,9,10)$$
(or)

12. Express the following in decimal
(a) $(10110.0101)_2$ (b) $(16.5)_{16}$ (c) $(26.24)_8$

13. What are SOP and POS forms of Boolean expressions? Obtain the minimal SOP expression for $\Sigma m(2,3,5,7,9,11,12,13,14,15)$ and complement it in NAND logic.
(or)

14. Reduce the following expressions using k-map and implement them in universal logic.
$$\Sigma m(5,6,7,9,10,11,13,14,15)$$

15. Design a 4 bit priority Encoder.
(or)

16. How will you build a 16 input MUX using only 4 input multiplexers.

17. With relevant diagrams and truthtable explain the operation of 4 – bit ripple counter.
(or)

18. Design following input sequence o1o1o11o1oo using the suitable logic.

19. Draw the circuit diagram of (a) CMOS inverter   (b)   CMOS NAND Gate and explain.
(or)

20. Draw the two dimensional addressing of RAM with block schematic.