

## III B.Tech I Semester Regular Examinations, November 2007

## DIGITAL IC APPLICATIONS

( Common to Electronics &amp; Communication Engineering and Electronics &amp; Instrumentation Engineering)

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions  
All Questions carry equal marks

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1. (a) Design CMOS transistor circuit for 3-input AND gate. With the help of function table explain the operation of the circuit diagram.
- (b) Design a CMOS transistor circuit that has the functional behavior as

$$f(x) = \overline{(a + \bar{b})(b + c)(a + \bar{c})}$$

Also draw the relevant circuit diagrams. [8+8]

2. (a) Design a transistor circuit of 2-input ECL NOR gate. Explain the operation with the help of function table.
- (b) A single pull-up resistor to +5V is used to provide a constant-1 logic source to 15 different 74LS00 inputs. What is the maximum value of this resistor? How much high state DC noise margin can be provided in this case? [8+8]
3. (a) Explain the various data types supported by VHDL. Give the necessary examples.
- (b) Discuss the case statement and its use in the VHDL program. [8+8]
4. Design a logic circuit to detect prime number of a 5-bit input. Write the structural VHDL program for the same. [16]
5. Design a two-digit BCD adder with logic gates. Using this logic write the VHDL program. In structural style of modeling. [8+8]
6. Design a combinational logic circuit that counts the number of ones in a 24-bit register. Write a VHDL program for the same using structural style or modeling. [16]
7. (a) Draw the logic diagram of 74×163 binary counter and explain its operation.
- (b) Design a modulo-100 counter using two 74×163 binary counters? [8+8]
8. (a) Design an 8×4 diode ROM using 74×138 for the following data starting from the first location.

6, 9, 0, C, D, 1, F, D

- (b) How many ROM bits are required to build a 16-bit adder/subtractor with mode control, carry input, carry output and two's complement overflow output. Show the block schematic with all inputs and outputs. [8+8]

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