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SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act,1956)

Course & Branch :B.E - EIE
Title of the Paper :Digital Logic Theory and Design Max. Marks :80
Sub. Code :6C0065 Time : 3 Hours
Date :10/11/2009 Session :FN

PART - A (10 x 2 = 20)

Answer ALL the Questions

1. Determine the decimal value of the fractional binary number 0.10101.
2. Prove that A + A'B = A + B
3. Define noise margin of a logic gate.
4. Show the logic diagram and truth table of a tri-state gate.
5. What do you mean by combinational circuit? Give examples.
6. Differentiate between PAL and PLA.
7. What do you mean by synchronous circuits? Give examples.
8. What is meant by race around condition in flip-flop?
9. Define state assignment.
10. What do you mean by cycles and races in asynchronous sequential circuit?

PART – B (5 x 12 = 60)

Answer All the Questions

11. Simply the expression
Y = ABCD + AB'CD + AB'C + AB. Convert this expression into a minterm SOP form and then simplify using Karnaugh Map.

(or)

12. (a) Perform l's complement and 2's complement addition for +45 and -35.
    (b) Simplify the expression
    $Y = \Sigma m (1, 4, 5, 7, 8, 9, 11)$ using Karnaugh map.

13. Draw and explain the circuit diagram of a basic totem-pole TTL NAND gate. Discuss about its characteristics and specification.

(or)

14. Draw and explain the circuit diagram of CMOS Inverter gate. Discuss about its characteristics and specification.

15. (a) Design a 3-to-8 decoder.
    (b) Implement $F(A, B, C, D) = \Sigma (0,1,2,5,7,11,15)$ using 8-to-1 multiplexer.

(or)

16. (a) Design a 4-bit binary-to-gray-code converter.
    (b) Design a full subtractor.

17. (a) Explain JK – FF with logic diagram, characteristic table and equation, present state-next state table, state diagram and application/excitation table.
    (b) Explain the realization of JK – FF from SR – FF.

(or)

18. Design and hence explain the working of a 4-bit ripple counter.

19. Design an synchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. Use JK FF for implementation of the circuit.

(or)

20. What are the hazards that occur in asynchronous sequential circuit? What are the ways in which they can be eliminated?