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SATHYABAMA UNIVERSITY

(Established under section 3 of UGC Act, 1956)

Course & Branch: B.E-EIE
Title of the Paper: Digital Logic Theory and Design Max. Marks: 80
Sub. Code: 6C0065 Time: 3 Hours
Date: 14/11/2010 Session: FN

PART - A (10 X 2 = 20)

Answer ALL the Questions

1. Convert decimal 58 to XS3 and to Gray.

2. State deMorgan's Theorems.

3. Compare two main features of TTL and CMOS logic gates.

4. What are tri-state gates?

5. Mention the types of adders.

6. Which gate is suitable for building a comparator and why?

7. Build a D flip-flop from SR flip-flop IC.

8. How are clocked sequential circuits used? Give an example.

9. What are pulse mode sequential circuits?

10. Define the racing condition.

PART – B (5 x 12 = 60)

Answer All the Questions

11. Determine the minimum expression for the following function F = Σ m (0,2,3,4,6,7,8,12,14,15,16,18,19,20,22,23,24,28) using any one standard method. Verify the result using tabular method.

(or)

12. (a) Simplify the Boolean expression – F = (((A'B'C)' _ A B)' (CB'))' and implement the same using Basic gates only, and then using NAND gates only Compare them.
    (b) Obtain the standard SOP and POS forms of F = A + BC'.

13. Discuss in brief about the digital logic families.

(or)

14. Write short notes on:
    (a) Tri state logic gates
    (b) Characteristics of ICL and CMOS logic gates.

15. What are Programmable Logic Devices? Write a descriptive note about them.

(or)

16. Design a Binary to BCD code converter.

17. With a neat sketch of the circuit describe a JK Master-Slave Flip-flop.

(or)

18. Design a mod – 5 synchronous counters.

19. Make short descriptions on:
    (a) States and output specifications
    (b) Race free assignments.

(or)

20. What are Hazards in sequential circuits? State their effects and also types. Discuss the salient features in detail.