ENGINEERING & MANAGEMENT EXAMINATIONS, DECEMBER - 2007

COMPUTER ARCHITECTURE & ORGANIZATION

SEMESTER - 5

Time : 3 Hours] [Full Marks : 70

GROUP - A

(Multiple Choice Type Questions)

1. Choose the correct alternatives for the following : 10 × 1 = 10

i) What is the 2's complement representation of – 24 in a 16-bit microcomputer ?

a) 0000 0000 0001 1000 b) 1111 1111 1110 1000

c) 1111 1111 1110 0111 d) 0001 0001 1111 0011. ☐

ii) The basic principle of the von Neumann computer is

a) storing program and data in separate memory

b) using pipeline concept

c) storing both program and data in the same memory

d) using a large number of registers. ☐

iii) In a microprocessor the address of the next instruction to be executed is stored in

a) stack pointer b) address latch

c) program counter d) general purpose register. ☐

iv) For BIOS (Basic Input / Output System) and IOCS (Input / Output Control System), which one of the following is true ?

a) BIOS and IOCS are same

b) BIOS controls all devices and IOCS controls only certain devices

c) BIOS is not a part of Operating Sysem and IOCS is a part of Operating System

d) BIOS is stored in ROM and IOCS is stored in RAM. ☐

v) The principle of locality justifies the use of

a) Interrupts b) Polling

c) DMA d) Cache Memory. [ ]

vi) The performance of a pipelined processor suffers if

a) the pipeline stages have different delays

b) consecutive instructions are dependent on each other

c) the pipeline stages share hardware resources

d) all of these. [ ]

vii) 'Delayed Branching' is related to

a) Pipeline hazard b) Pipeline remedy

c) both (a) and (b) d) none of these. [ ]

viii) How many RAM chipes of size (256 × 1 bit) are required to build 1 M byte memory ?

a) 8 b) 10

c) 24 d) 32. [ ]

ix) The mode field determines

a) the type of addressing

b) the type of operand

c) the type of instruction format

d) the type of arithmetic or logic operation. [ ]

x) By left-shifting the content of a register once, its content is

a) doubled b) halved

c) both (a) and (b) d) no such decision can be made. [ ]

GROUP – B

(Short Answer Type Questions)

Answer any *three* of the following. 3 × 5 = 15

2. What is Harvard Architecture ? Explain briefly using a block diagram. 1 + 4

3. Sketch the instruction format of a two address instruction that uses immediate, register direct and indexed addressing mode if size of the memory is 1 MB and size of instruction word is limited to 16 bits with 3 bit opcode field. 5

4. What is flash memory ? Explain with an example. 2 + 3

5. What are the advantages of relative addressing mode over direct addressing mode ? 5

6. Distinguish between arithmetic pipeline and instruction pipeline. 5

GROUP – C

(Long Answer Type Questions)

Answer any *three* of the following questions. 3 × 15 = 45

7. a) With the help of a block diagram discuss the construction and working of a 8 bit carry-look-ahead adder. Also compute total time needed to perform one addition using gate delay of each gate δ μs and no delay are involved in the connecting wires. 8 + 3

   b) What are the advantages of carry-look-ahead adder over ripple-carry adders ? Explain. 4

8. a) Using Booth's algorithm, multiply (+ 14) and (– 12) when the numbers are represented in 2's complement form. 9

   b) Compare and contrast restoring and non-restoring divisions. 6

9. a) Explain Flynn's classification for multi-processor system. 5

   b) Discuss the advantages of vector processing over scalar processing. 5

   c) Explain how daisy chaining is used for bus arbitration in a multiprocessor system. 5

10. a) What is meant by 'Pipeline architecture' ? 2

b) How does it improve the speed of execution of processor ? 5

c) What are pipeline hazards ? 3

d) A non-pipeline system takes 40 ns to process a task. The same task can be processed in a four segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 50 tasks. What is the maximum speed up that can be achieved in this case ? 5

11. Write short notes on any *three* of the following : 3×5

a) Microprogramming and microprogrammed control unit

b) Page replacement policies

c) Interrupt servicing with priority interrupts

d) Vector processors and their uses

e) Architecture of 10 P.

END