Code: AE09

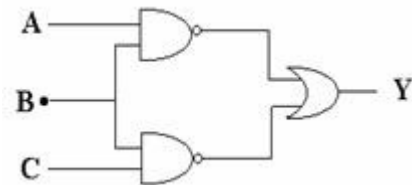**Subject: ANALOG & DIGITAL ELECTRONICS**
Time: 3 Hours
Max. Marks: 100

NOTE: There are 9 Questions in all.
* **Question 1 is compulsory and carries 20 marks. Answer to Q. 1. must be written in the space provided for it in the answer book supplied and nowhere else.**
* **Out of the remaining EIGHT Questions answer any FIVE Questions. Each question carries 16 marks.**
* **Any required data not explicitly given, may be suitably assumed and stated.**

Q.1   Choose the correct or best alternative in the following:
    (2x10)

   a.   A PLA can be used

   (A) as a microprocessor logic.   **(B)** a combinational logic.
   (C) a sequential logic.   **(D)** None of above.

   b. For the logic circuit shown the O/P Y is equal to

   (A) $\overline{ABC}$.
   (B) $\overline{\overline{A} + \overline{B} + C}$.
   (C) $\overline{A} + \overline{B} + \overline{C}$.
   (D) $\overline{\overline{AB} + \overline{BC}}$.

   c. Which one is the fastest logic family

   (A) ECL.   **(B)** TTL.
   (C) NMOS.   **(D)** T^2L

   d. If each input voltage is amplified by a different factor at the output then the opamp circuit is called as

(A) Averaging amplifier.　　　　　(B) Summing amplifier.
(C) Scaling amplifier.　　　　　　(D) Differential amplifier.

e. The input resistance of 741 op-amp is

(A) 10 MΩ.　　　　　　　　(B) 1 MΩ.
(C) 100 Ω.　　　　　　　　(D) 1 KΩ.

f. The ratio of change in input offset voltage when variation in supply voltage is made, is called _____

(A) SVRR　　　　　　　　　　(B) Slew rate
(C) CMRR　　　　　　　　　　(D) Voltage gain

g. A 1:16 demultiplexer has following features

(A) 1 I/P, 16 O/P's, 4 control signals.
(B) 2 I/P, 8 O/P's, 2 control signals.
(C) 2 I/P, 8 O/P's, 2 strobe signals.
(D) 16 O/P's.

h. Unity gain bandwidth Product of 741 op-amp is

(A) 4 MHz　　　　　　　　　(B) 6 MHz
(C) 1 MHz　　　　　　　　　(D) 100 Hz

i. A notch filter is a

(A) Wide band pass filter　　　　(B) Narrow band pass filter
(C) Wide band reject filter　　　(D) Narrow band reject filter

j. The number of flip flop required to construct MOD-7 counter that counts from 0 to 6 is

(A) 4.　　　　　　　　　　　(B) 3.
(C) 2.　　　　　　　　　　　(D) 1.

Answer any FIVE Questions out of EIGHT Questions.
Each question carries 16 marks.

Q.2 a. Explain the factors that determines the operating speed of Logic gate. Discuss, how the speed performance can be improved in Schottky TTL transistors. **(8)**

b. Write the various features of ECL family and draw the basic ECL logic NOR gate and explain it.
(8)

Q.3 a. Explain the architecture of 741 op-amp? Discuss the operation of each block?
(8)

b. Draw the circuit of a MOS operational amplifier & explain its operation.
(8)

Q.4 a. Compare and contrast a programmable logic array with a programmable array logic (PAL). **(6)**

b. Write the acronyms EPROM & E^2PROM. **(2)**

c. What do you mean by priority encoder and explain the priority encoder for 10 line decimal to 4 line BCD with its truth table? **(8)**

Q.5 a. What is race around condition in JK flip flop? How this condition will be overcome? **(8)**

b. Explain how shift register can be used as
(i) serial to parallel data converter, and (ii) parallel to serial data converter.
(8)

Q.6 a. What are the different types of A/D converter? Explain the converter, which is designed to convert analog wave form into binary code. **(8)**

b. Explain Dual slope converter. Discuss the advantages & disadvantages of Dual slope converter. **(8)**

Q.7 a. What types of MOSFET is used in CMOS logic family? Mention its advantages & disadvantages with a neat sketch. Also describe the CMOS NOR gate. **(12)**

b. Draw the circuit symbol for transmission gate? Explain the operation of transmission gate in short. **(4)**

Q.8 a. Explain how switched capacitor filter behaves as a resistance with a circuit diagram. **(8)**

b. Determine the order of 1-dB ripple Chebyshev filter that gives a 40 dB attenuation at $\omega/\omega_c = 2$. Determine the 3-dB bandwidth of the filter. **(8)**

Q.9 Write short notes on any **TWO** of the following:

(i) N-MOS logic circuits.
(ii) log and antilog amplifiers.

(iii)   Digital comparator.
(iv)   Seven   segment   display   system.
   (8+8)